(12)特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2000 年11 月30 日 (30.11.2000)

PCT

(10) 国際公開番号
WO 00/72376 A1

(51) 国際特許分類7: H01L 21/68, B23Q 3/15, H02N 3/15

(21) 国際出願番号: PCT/JP00/03355

(22) 国際出願日: 2000 年5 月25 日 (25.05.2000)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願平11/145507 1999 年5 月25 日 (25.05.1999) JP

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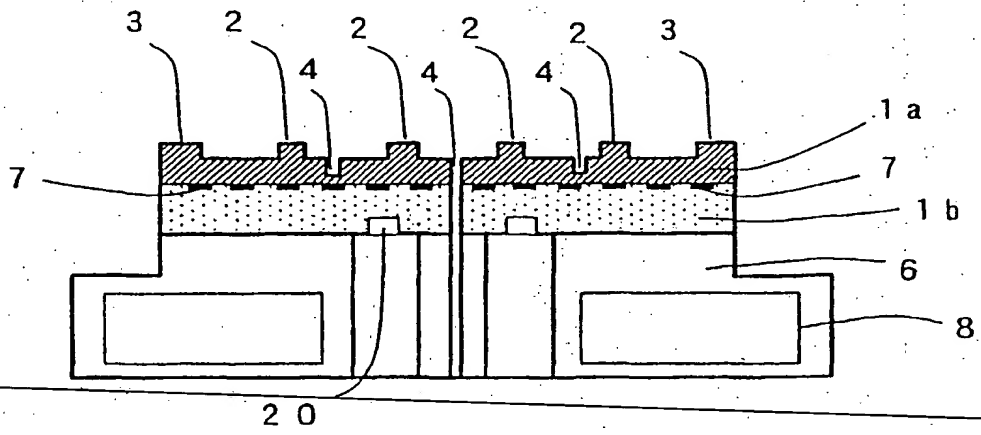
(81) 指定国 (国内): AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD.

/続葉有/

(54) Title: ELECTROSTATIC CHUCK AND TREATING DEVICE

(54) 発明の名称: 静電チャックおよび処理装置



(57) Abstract: An electrostatic chuck for insulating substrate attraction, comprising a dielectric substrate (1a) acting on one surface thereof as an attraction surface of an insulating substrate and provided on the other surface with a plurality of electrodes (7) in order to electrostatic-attracting an insulating substrate such as a glass substrate, an insulating support base (1b) for fixing the dielectric substrate, a plurality of conducting terminals provided on the insulating support base, and a means for electrically connecting the electrodes with the conducting terminals, wherein a resistivity at room temperature of the dielectric substrate is up to 10^{13} Ωcm, a thickness of the dielectric substrate up to 2 mm, a width of an electrode up to 4 mm, and an interval between electrodes up to 2 mm. A heating/cooling plate (6), a gas supply piping for supplying gas to a gap between the insulating substrate and the attraction surface, and a temperature control system for controlling the temperature of the insulating substrate are added to the above electrostatic chuck for insulating substrate attraction to constitute an insulating substrate treating device.

/続葉有/

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明細書

静電チャックおよび処理装置

技術分野

本発明はＰＤＰ（プラズマディスプレー）製造装置、ＤＶＤ（デジタルビデオディスク）マスタライタ製造装置、ハードディスク製造装置に使用される基板処理装置及びＥＢ（エレクトロンビーム）露光装置におけるレチクル固定装置、更にＳＯＳ（シリコンオンサファイア）やＳＯＩ（シリコンオンインシュレータ）ウェハ上に形成される素子を製造するＣＶＤ、エッチング装置やスパッタリング装置に使用される絶縁性基板処理装置に関するものである。

背景技術

ＤＶＤやＰＤＰ製造装置等においては、被処理体がガラス基板であり電気絶縁性を示す。そのため従来はこれらの基板を真空中で静電吸着することができずその製造装置においてステージ上に平置きされたり、機械的な機構により固定され処理されていた。

ＥＢ露光機のレチクルは石英製であり同様に電気絶縁性を示す。そのため真空下でレチクルを固定するために従来は機械的な機構により固定されていた。

シリコンウェハの次世代代替品として注目されているＳＯＳ基板やＳＯＩ基板はステージ載置面が電気絶縁性を示す。そのため従来はこれらのウェハ上に素子を形成する製造装置においてシリコンウェハの場合のような静電チャックを用いた固定方法を採用することができなかった。シリコンウェハを静電吸着する手段および原理は特開平５－６３０６２に開示されているがその原理によると絶縁性基板は静電吸着することができない。

また静電プロッタのように紙を静電気的に吸引する装置があった。

請求の範囲第１１項～第１３項は前記静電チャックを用いた減圧下での絶縁性基板の処理方法を開示した。

請求の範囲第１４項～第１５項は前記静電チャックにプロセスによって発生する熱や、絶縁性基板に供給する熱を媒体によって供給または放散させるための流路を設けたプレートと、絶縁性基板と誘電体吸着面間の隙間の熱伝達を調整するために封止するガスを供給するためのガス供給配管、及び絶縁性基板の温度によって前記の封止するガス圧力を調整し予め設定した温度に調節が可能になる絶縁性基板加熱冷却装置及び温度制御システムを開示した。

図面の簡単な説明

図１は、静電チャックの一例を示す平面図である。

図２は、Ａ－Ａに沿った図１の断面図である。

図３は、静電チャックにより絶縁性基板を吸着した別実施例の断面図である。

図４は、誘電体に設けられた電極のパターン例である。

図５は、誘電体に設けられた電極のパターン例である。

図６は、誘電体に設けられた電極のパターン例である。

図７は、加熱冷却ガス圧力と絶縁性基板の温度との関係を示すグラフである。

図８は、静電チャックの印可電圧と絶縁性基板の温度との関係を示すグラフである。

図９は、静電チャックの固体接触部の面積比率と絶縁性基板の温度との関係を示すグラフである。

発明を実施するための最良の形態

本発明の好適な実施例を図を用いて説明する。図１は本発明に係る静電チャックの一例を示す平面図であり、図２はその断面図である。

図３は絶縁性支持基盤１ｂを誘電体基板１ａと同質の材料とし積層構造にすることで一体化した実施例であり、静電チャック１に絶縁性基板１０を吸着した

【表１】

NO	本発明の範囲	誘電体材料	被吸着体	厚さ（μm）	誘電体の抵抗率（Ωcm）	誘電体の比誘電率	誘電体の表面粗さ Ra（μm）	静電吸着力（g/5cm²）
1A	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm、比誘電率5	500	10^{10}	9	0.25	>300
1B	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{11}	9	0.25	>300
1C	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{12}	9	0.25	>300
1D	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{13}	9	0.25	>300
1E	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	1000	10^{11}	9	0.25	>300
1F	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{11}	9	0.4	250
1G	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{11}	9	1.0	50
1H	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	石英ガラス、厚さ5mm、比誘電率4	500	10^{11}	9	0.25	>300
1I	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	サファイア、厚さ0.5mm、比誘電率10	500	10^{11}	9	0.25	>300
1J	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	高誘電体基板（比誘電率120、厚さ0.5mm）	500	10^{11}	9	0.25	>300
1K	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	高誘電体基板（比誘電率10000、厚さ0.5mm）	500	10^{11}	9	0.25	>300
1L	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	ポリイミドフィルム（厚さ50μm）	500	10^{11}	9	0.25	100
1M	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	SOIウェハ	500	10^{11}	9	0.25	>300
1N	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	SOSウェハ	500	10^{11}	9	0.25	>300
1O	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	多結晶アルミナ基板、厚さ0.6mm、表面粗さRa0.1μm、比誘電率10	500	10^{11}	9	0.25	>300
1P	○	Al2O3-Cr2O3-TiO2セラミックス焼結体	多結晶アルミナ基板、厚さ0.6mm、表面粗さRa0.4μm、比誘電率10	500	10^{11}	9	0.25	>300
2	○	Al2O3セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{15}	9	0.1	100
3	○	BaTiO3セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{11}	120	0.1	150
4	○	BaTiO3セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{10}	10000	0.2	100
5	○	BaTiO3セラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{9}	20000	0.3	100
6	○	SiCセラミックス焼結体	低アルカリガラス、基板厚さ0.6mm	500	10^{10}	120	0.1	>300
7	○	シリコンゴム	低アルカリガラス、基板厚さ0.6mm	500	10^{10}	3	0.4	150

るほど被吸着体の表面粗さが粗くできることがわかった。

誘電体の材料をかえたときの静電吸着力を２～７に示した。アルミナに酸化クロム、酸化チタンを添加したセラミックス焼結体以外でも静電吸着することが示された。被吸着体がＰＤＰ用ガラスの場合は、その視認性の点からもガラスに傷が入りにくいゴム系の材料が有効である。本実施例ではシリコンゴムを用いたが天然ゴム、クロロプレンゴム、ブチルゴム、ニトリルゴム、フッ素ゴム更にポリウレタン、ＰＴＦＥ等の樹脂であっても良い。この場合体積抵抗率が$10^{13}\Omega$ｃｍ以下が望ましい。

表２は、アルミナに酸化クロム、酸化チタンを添加したセラミックス焼結体からなる材料を用い、本発明にかかる静電チャックの電極パターンを変えたときのガラス基板の静電吸着力と印可電圧（１０ＫＶ印可）との関係である。

同一の電極巾、電極間距離のパターンでは誘電体の厚さは０．３ｍｍがもっとも静電吸着力が大きく、薄くすれば静電吸着力が大きくなる傾向にある。

電極巾、間隔とも０．５ｍｍ以上であれば静電吸着力が可能であることがわかったが、電極間隔が０．５ｍｍより狭い場合は電極間の絶縁が十分得られなくなり結果として静電吸着できない場合もあった。

同一誘電体厚さで比較すると電極巾が狭いほど大きな静電吸着力が得られた。

電極間距離が２ｍｍより大きい場合はほとんど静電吸着力が得られなかった。今回の試験では印可電圧を１０ＫＶまで印可したが更に大きな電圧を印可すれば電極間距離２ｍｍでも静電吸着力が発現することが期待される。

同一誘電体厚さ、同一電極巾で比較すると電極間隔が誘電体の厚さより大きくなると静電吸着力が小さくなる傾向にあった。

以上をまとめると、誘電体の厚さは薄く、電極の巾は狭く、電極間は電極の巾と同程度である場合に大きな静電吸着力が得られることがわかった。

被吸着体としてガラス基板を静電吸着する場合は誘電体厚さは０．３ｍｍ～２．０ｍｍ、電極間隔が０．５～１ｍｍ以下、電極巾は０．５ｍｍ～４ｍｍ、誘電体の抵抗率$10^{13}\Omega$ｃｍ以下で実用化できるが、更により好ましくは誘電体厚さは０．３ｍｍ～１．０ｍｍ、電極間隔が０．５～１ｍｍ以下、電極巾は０．５ｍｍ～１ｍｍ、誘電体の抵抗率$10^{13}\Omega$ｃｍ以下が望ましい。

次に基板加熱冷却装置の実施例について記載する。

図７～９は各種熱吸着試験データおよび絶縁性基板冷却試験特性の実験データを示すグラフであり、各グラフの説明を以下に示す。絶縁性基板１０は、ガラス基板（低アルカリガラス）を用いた。

図７は真空チャンバ内に設置した基板加熱冷却装置に絶縁性ガラス基板を設置し、絶縁性基板の温度と絶縁性基板と誘電体吸着面の間隙に供給される加熱冷却用ガスの圧力との関係である。絶縁性基板１０の上面から２W/cm^2の熱流を与えたときの熱特性を、横軸に上記ガスの圧力、縦軸に絶縁性基板１０の表面温度として表した。ガス封入部９のガス圧力を変化させることで絶縁性基板１０の温

非常に大きい静電チャックが必要となる。ここでは静電チャックの絶縁層の材料としてアルミナを主成分とし、酸化クロム（Cr_2O_3）、酸化チタン（TiO_2）および焼結助材を適量添加したセラミック焼結体を用いた。この材料の吸着力は１Ａ～１Ｃと同じく１０ＫＶ印可で約３００g/５cm^2であり垂直方向の引張り強度が３００ｇ／cm^2と推定される。接触面積比率が２０％であっても６０g/cm^2以上が確保でき十分に絶縁性基板を吸着できる。

本実施例では、絶縁性基板１０として、低アルカリガラス基板を用いたが、本発明の静電チャックは、電気絶縁性基板およびフィルム一般に適用できる。

また絶縁性基板加熱冷却装置の絶縁性支持基盤内にヒーターを設け、被吸着体を測温する手段として光温度計、熱電対、その他非接触温度計を設けその計測器から出力される信号と予め設定した値とを比較することにより被吸着体の温度制御が容易になる。また絶縁性基板を直接測温できない場合は予め蓄積されたガス圧力、印可電圧、固体接触面積比率、入射熱エネルギー、媒体流量、媒体温度等の関連を記載されたデータベースに基づき絶縁性基板の温度を一定に保つ調整が可能になる。

本実施例で開示した絶縁性基板加熱冷却装置を反応チャンバ内に設置することにより、ＳＯＳやＳＯＩウェハのプラズマＣＶＤ、プラズマエッチングやスパッタリング等の半導体製造プロセスでの温度管理が非常に容易になる。

産業上の利用可能性

以上に説明した如く本発明によれば、被処理体が絶縁体である場合も静電チャックを用いて吸着することができるため、静電チャックを組み込んだ加熱冷却装置を用いれば絶縁性基板の加熱、冷却が容易になり絶縁性基板を所定の温度に制御することが可能となる。

ことを特徴とする請求の範囲第１項～第７項のいずれか１項に記載の静電チャック。

９．　前記導電性端子は、前記絶縁性支持基盤にロウ付け、はんだ付け、導電性接着剤のいずれかによる接着により設けられていることを特徴とする請求の範囲第１項～第８項のいずれか１項に記載の静電チャック。

１０．　前記電気的接続手段は、導電性ワイヤー、導電性棒、導電性樹脂充填、ハンダ充填のいずれかによることを特徴とする請求の範囲第１項～第９項のいずれか１項に記載の静電チャック。

１１．　一方の面が絶縁体基板を吸着する吸着面とし、もう一方の面に複数の電極が設けられた誘電体基板と、前記誘電体基板を固定する前記絶縁性支持基盤と、該絶縁性支持基盤に設けられた複数の導電性端子と、前記誘電体基板に設けられた複数の電極と、前記導電性端子とを各別々に電気的に接続する手段と、高圧電源と、高圧電源と前記複数の導電性端子とを電気的に接続する手段と、を有し、前記吸着面に載置された絶縁性基板を静電吸着することを特徴とする絶縁性基板静電吸着処理方法。

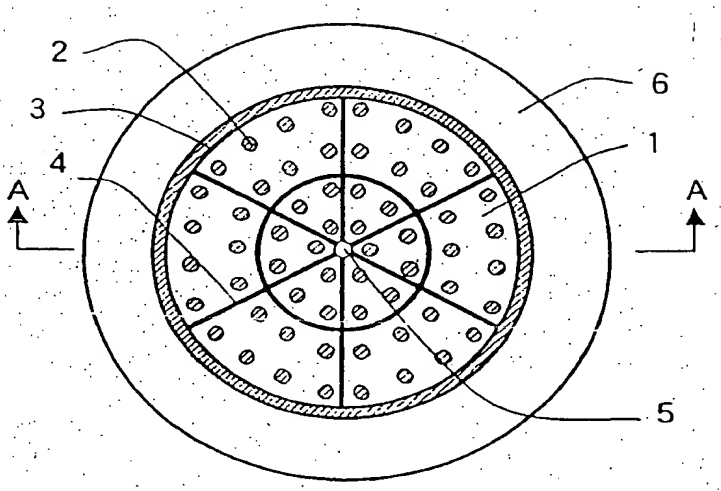
１２．　真空減圧下で処理することを特徴とする請求の範囲第１１項記載の絶縁性基板静電吸着処理方法。

１３．　絶縁体である被処理基板を静電吸着し、被処理基板と誘電体吸着面との間に形成された隙間空間内に、被処理基板の加熱・冷却を行うガスを封入し、該ガスの圧力領域が、分子流領域であることを特徴とする請求の範囲第１１項または第１２項に記載の絶縁性基板静電吸着処理方法。

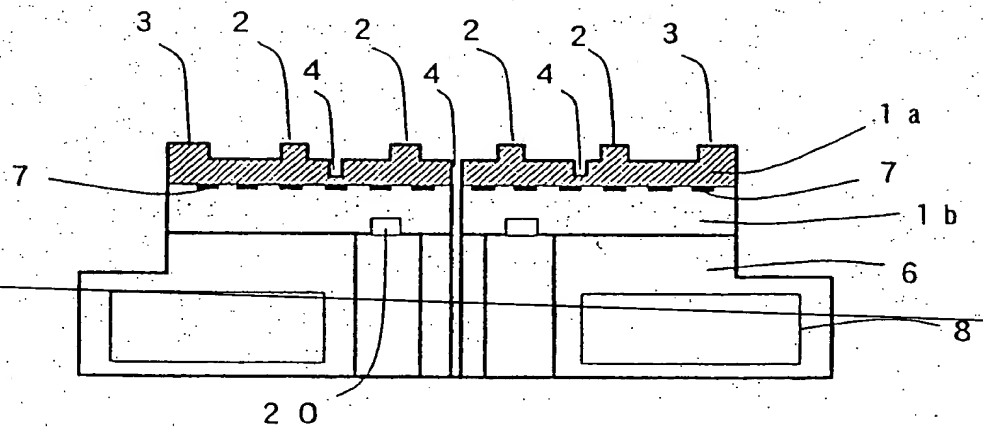
１４．　請求の範囲第１項～第１０項のいずれかに記載の静電チャックと、該静電チャックを支持するための媒体流路が内蔵されているプレートと、該静電チャックと該プレートとを接着する手段と、からなる絶縁性基板加熱冷却処理装置。

１５．　請求の範囲第１項～第１０項のいずれかに記載の静電チャックと、該静電チャックを支持するための媒体流路が内蔵されているプレートと、静電チャックと該プレートとを接着する手段と、誘電体および絶縁性支持基盤およびプレー

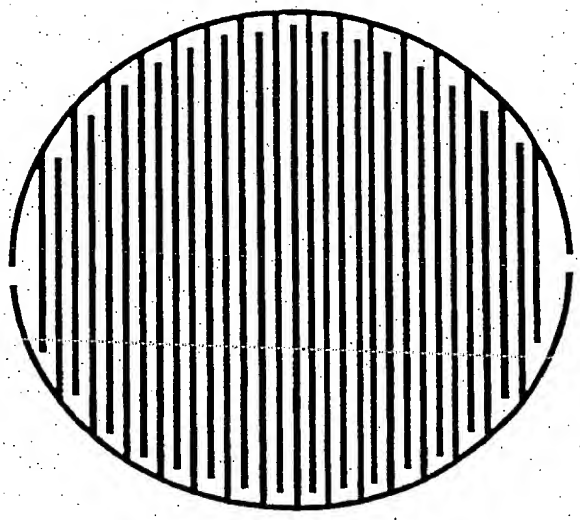
【図１】



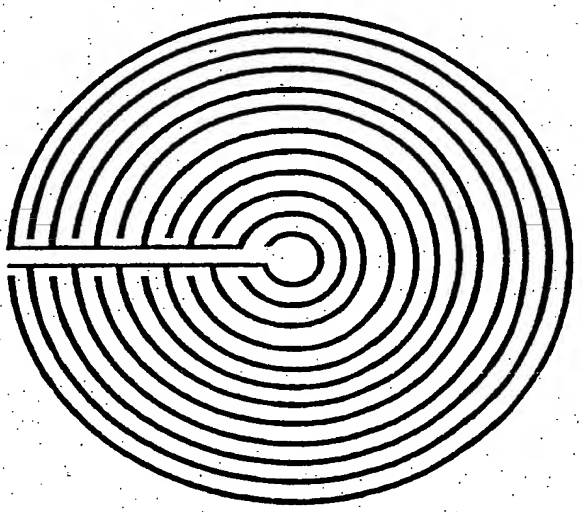
【図２】



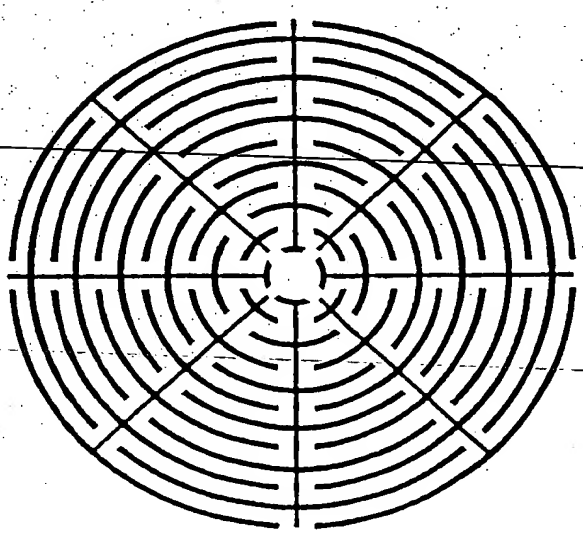
【図４】



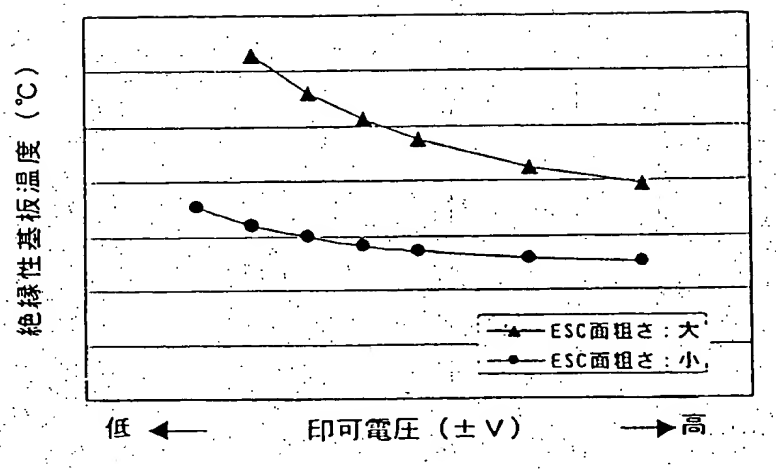
【図５】



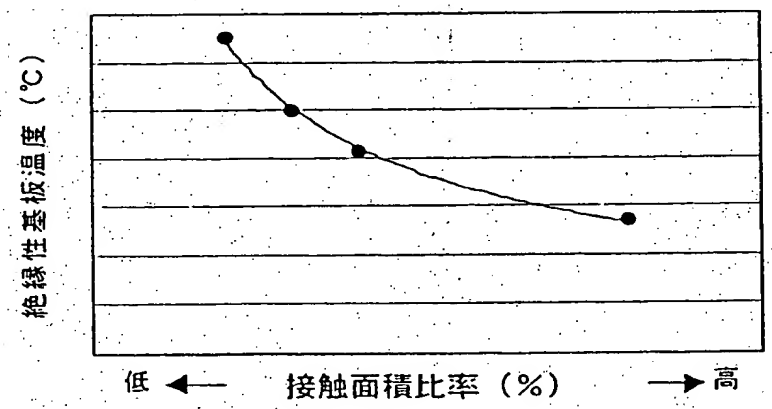
【図６】



【図８】



【図９】



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/03355

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Figs. 10, 11, 15 to 19 & US, 5810933, A & JP, 9-232415, A & TW, 300312, A & KR, 97063549, A & SG, 69168, A	
Y	JP, 10-223742, A (Kyocera Corporation), 21 August, 1998 (21.08.98), Claims; Par. Nos. [0001], [0020] to [0029]; Fig. 2 (Family: none)	6-10, 14-16
Y	EP, 803904, A (APPLIED MATERIALS,INC.), 29 October, 1997 (29.10.97), page 3, lines 29-49; page 6, lines 35-39; page 6, lines 55-56; page 7, lines 3-21; Figs. 1, 3 to 5, 7 & US, 5761023, A & JP, 10-41378, A	13,16
Y	JP, 9-17770, A (Sony Corporation), 17 January, 1997 (17.01.97), Par. Nos. [0028] to [0029]; Fig. 1 (Family: none)	14,16

国際調査報告

国際出願番号　PCT／JP00／03355

C（続き）．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP，11－8291，A（株式会社日立製作所），12．1月．1999（12．01．99），段落【0014】－【0019】（ファミリーなし）	3－10，14－16
Y	JP，5－211228，A（東陶機器株式会社），20．8月．1993（20．08．93），特許請求の範囲＆TW，236709，A	4－10，14－16
Y	EP，790641，A（Novellus Systems，inc．），20．8月．1997（20．08．99），第7頁第9行－同頁第23行，第9頁第14行－第10頁第18行，第10図，第11図，第15図－第19図＆US，5810933，A＆JP，9－232415，A＆TW，300312，A＆KR，9706354 9，A＆SG，69168，A	5－10，14－16
Y	JP，10－223742，A（京セラ株式会社），21．8月．1998（21．08．98），特許請求の範囲，段落【0001】，段落【0020】－【0029】，第2図（ファミリーなし）	6－10，14－16
Y	EP，803904，A（APPLIED MATERIALS，INC．），29．10月．1997（29．10．97），第3頁第29行－同頁第49行，第6頁第35行－同頁第39行，第6頁第55行－同頁第56行，第7頁第3行－同頁第21行，第1図，第3図－第5図，第7図＆US，5761023，A＆JP，10－41378，A	13，16
Y	JP，9－17770，A（ソニー株式会社），17．1月．1997（17．01．97），段落【0028】－【0029】，第1図（ファミリーなし）	14，16

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 791 956 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.08.1997 Bulletin 1997/35

(51) Int Cl.6: H01L 21/68, H01L 21/00

(21) Application number: 96306414.2

(22) Date of filing: 04.09.1996

(84) Designated Contracting States:
DE FR GB

(30) Priority: 06.09.1995 JP 229190/95
20.08.1996 JP 218259/96

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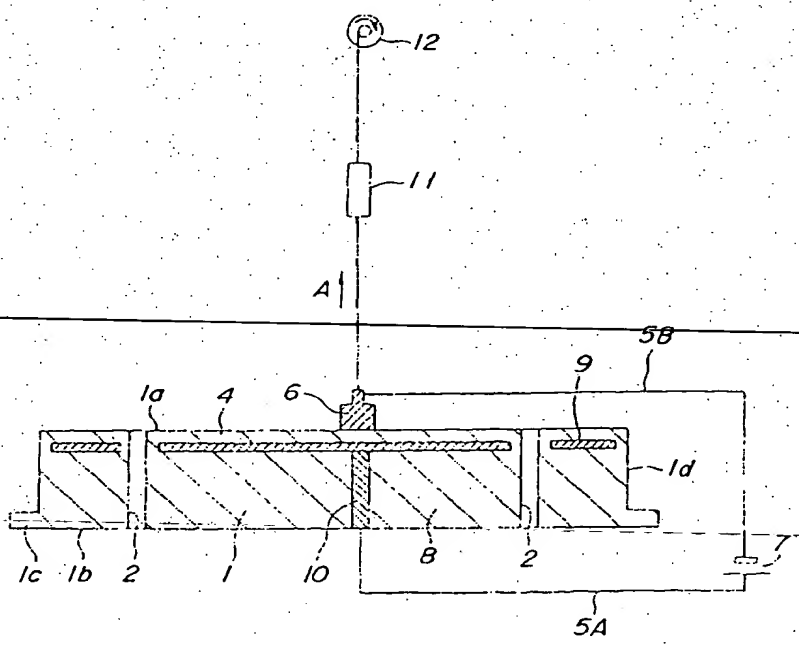
(54) Electrostatic chuck

(57) An electrostatic chuck for attracting an object to be treated, includes a substrate(1), an insulating dielectric layer (4) and at least one electrode (9) provided between the substrate and the insulating dielectric layer, wherein the above object is to be attracted onto the electrode via the insulating dielectric layer and an average thickness of the insulating dielectric layer (4) is not less than 0.5 mm and not more than 5.0 mm.

FIG_2



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requirements. Japanese Utility Model Registration Application Laid-open No. 2-120.531 also suffer the above problems.

In view of the above, the present inventors produced insulating dielectric layers having thicknesses of a few tens μm to 300 μm from various ceramic materials, and examined them with respect to attracting force and leakage current. In general, in order to exhibit sufficiently high attracting force, the insulating dielectric layer needs to have a volume resistivity of 1×10^{13} Ω·cm or less in a use temperature range.

It was clarified that an electrostatic chuck having an insulating dielectric layer with a volume resistivity, for example, in a range of 1×10^{11} to 1×10^{13} Ω·cm at room temperature exhibited high attracting force in a range of room temperature to 200°C, but leakage current largely increased at temperatures of more than 200°C, which might damage a semiconductor wafer. It was also clarified that the electrostatic chuck having the insulating dielectric layer with the volume resistivity of 1×10^{14} Ω·cm to 1×10^{16} Ω·cm at room temperature had a high attracting force in a temperature range of 100°C to 500°C, but its leakage current largely increased when the temperature was more than 500°C so that the semiconductor wafer might be damaged. It was further clarified that in the electrostatic chuck with the insulating dielectric layer having the volume resistivity of 1×10^{9} Ω·cm to 1×10^{10} Ω·cm at room temperature exhibited high attracting force in a temperature range of -20°C to 100°C, but it damaged the semiconductor wafer due to largely increased leakage current at temperatures of more than 100°C.

In this way, it was clarified that although the conventional ceramic electrostatic chucks all exhibited sufficiently high attracting forces in an optimum temperature range, the leakage currents largely increased if the use temperature rose and the volume resistivity of the insulating dielectric ceramic layer decreased to 10^{9} Ω·cm or less. Therefore, it was clarified that the conventional electrostatic chucks had a problem in such a use in which a use temperature range is wide, for example, in such a case where various treatments are effected for semiconductor wafers chucked.

Further, in Japanese Utility Model Registration Application Laid-open No. 2-120831, heat needs to be conducted between the semiconductor wafer and the electrostatic chuck uniformly as viewed planarly from the attracting surface thereof. For, even if the temperature of the attracting surface of the electrostatic chuck is equal, a large difference in temperature of the surface of the wafer occurs between a helium gas-filled portion and a helium gas non-filled portion inside the grooves. Consequently, the quality of the resulting semiconductor film varies, which may cause unacceptable products during the production process. Therefore, it is necessary to keep the pressure of the helium gas constant in every portion inside the grooves.

However, in the locations of the actual attracting chuck from which helium gas is to be fed are limited, and their feed openings of the helium gas-feeding locations are away from adjacent ones. Therefore, as the location goes away from a blow-out opening of the helium gas, the pressure of the gas rapidly decreases. In particular, as mentioned above, the thickness of the insulating dielectric layer is merely around a dozen μm to 300 μm, and the insulating dielectric layer merely has a minimum thickness required to maintain a necessary dielectric breakdown strength. This dielectric breakdown strength is a value of a minimum thickness portion of the insulating dielectric layer. For these reasons, the thickness of the grooves must inevitably be set at a few μm to a dozen μm. However, the grooves having a depth of a few μm to a dozen μm gives a large resistance against diffusion of the gas, so that the gas is not sufficiently diffused. Consequently, a large pressure difference occurs inside the grooves and the temperature varies in the semiconductor wafer, so that the quality of the film formed becomes non-uniform. Simultaneously with this, increase in the depth of the grooves causes antonymy that dielectric breakdown may occur between the grooves and the electrode.

Summary of the Invention

It is an object of the present invention to provide an electrostatic chuck for attracting an object to be treated, which can reduce leakage current in a insulating dielectric film to prevent an adverse effect upon the object and simultaneously to maintain the attracting force for the object high, even in a case where the electrostatic chuck is used in a temperature range in which the volume resistivity of the insulating dielectric film is decreased.

It is another object of the present invention to provide an electrostatic chuck for attracting an object to be treated, which can reduce difference in pressure of the gas inside grooves to uniformly conduct heat between every portion of the object and the attracting surface of the electrostatic chuck and simultaneously with this, to reduce the possibility of the dielectric breakdown as small as possible, in a case where a gas introducing hole is provided to be opened at the attracting face of the insulating dielectric layer of the electrostatic chuck and the gas is fed to the grooves or concaves of an attracting face side.

The electrostatic chuck according to the present invention is to attract an object to be treated, and comprises a substrate, an insulating dielectric layer and an electrode provided between the substrate and the insulating dielectric layer, wherein said object is to be attracted onto the electrode via the insulating dielectric layer and the average thickness of the insulating dielectric layer is not less than 0.5 mm and not more than 5.0 mm.

Another electrostatic chuck according to the present invention is to attract an object to be treated, and comprises a substrate, an insulating dielectric layer and an electrode provided between the substrate and the insulating dielectric layer, wherein said object is to be attracted onto the electrode via the insulating dielectric layer, a gas-introducing hole

peel off from the chuck even when a gas at pressure of 10 to 20 torr was flown between the semiconductor wafer and the attracting face of the chuck in an ordinary manner. It was also discovered that similar results were obtained even at not less than 500°C for the electrostatic chuck with the insulating dielectric layer having the volume resistivity of 1 x 10^{14} Ω·cm to 1 x 10^{16} Ω·cm at room temperature. Furthermore, it was discovered that similar results were obtained even at not less than 100°C for the electrostatic chuck with the insulating dielectric layer having the volume resistivity of 1 x 10^{9} Ω·cm to 1 x 10^{10} Ω·cm at room temperature.

As mentioned above, it was confirmed that excellent attracting force can be obtained in the electrostatic chuck with the insulating dielectric layer having such a large thickness as the skilled person in the art has not considered, and that the leakage current can be simultaneously largely reduced.

In addition, if the electrostatic chuck is used for a semiconductor-producing apparatus, the chuck is exposed to a halogen based corrosive gas as an etching gas or a cleaning gas. In a process such as sputtering, CVD or etching, the chuck is exposed to plasma. If the insulating dielectric layer made of even a ceramic material is subjected to the halogen based corrosive gas, a reaction product is produced on its surface, and dielectric breakdown may occur starting from any point in a layer of the reaction product through use for a long time under exposure to the plasma. The dielectric breakdown can be assuredly prevented by setting the thickness of the insulating dielectric layer at not less than 500 μm from the standpoint of the corrosion resistance and the plasma resistance.

According to the present invention, the leakage current is more conspicuously reduced by setting the thickness of the insulating dielectric layer at not less than 1.0 mm, whereas the above attracting force is further enhanced by setting the thickness of the insulating dielectric layer at not more than 3.0 mm.

Further, according to the electrostatic chuck of the present invention, the surface roughness, Rmax, of the surface of the insulating dielectric layer is preferably not more than 3 μm. By so doing, the attracting force is particularly increased. If the surface roughness, Rmax, of the insulating dielectric layer is not less than 4 μm, the attracting force is not almost increased even if the voltage applied to the electrodes is increased, whereas if the surface roughness, Rmax, is not more than 3 μm, the attracting force is not only largely increased, but also the attracting force sharply varies to response the increase in the voltage applied to the electrodes.

Further, if the maximum pore diameter of the insulating dielectric layer is set at not more than 5 μm, the surface roughness, Rmax, thereof can be controlled to not more than 3 μm, whereas if the maximum pore diameter is more than 5 μm, the surface roughness, Rmax, of the surface of the insulating dielectric layer could not be controlled to not more than 3 μm even if the surface was finely polished.

The porosity of the insulating dielectric layer is preferably not more than 3 %. For, it was clarified that if the thickness of the insulating dielectric layer falls in the range of the present invention and the surface roughness, Rmax, is set at not more than 3 μm, the attracting force can be most enhanced, when the porosity is not more than 3 %. It was further clarified that if the porosity is more than 3 %, the attracting force was not conspicuously enhanced even if the thickness and Rmax of the insulating dielectric layer are controlled to the above-mentioned respective ranges, the attracting force could not be conspicuously enhanced.

The electrostatic chuck according to the present invention with the insulating dielectric layer having the volume resistivity of not more than 1 x 10^{13} Ω·cm can afford high attracting force, and can be favorably used in practice. Particularly, when the volume resistivity of the insulating dielectric layer is even in a range of not more than 1 x 10^{9} Ω·cm to not less than 1 x 10^{7} Ω·cm, sufficiently high attracting force can be obtained, and leakage current can be conspicuously reduced.

The volume resistivity of the insulating dielectric layer is more preferably set at not less than 1 x 10^{8} Ω·cm from the standpoint of the reduction in the leakage current. However, if the leakage current up to about 10 mA is acceptable with respect to an 8-inch wafer, excellent effects can be obtained according to the present invention even if the volume resistivity of the insulating dielectric layer is in a range of 1 x 10^{7} Ω·cm to 1 x 10^{8} Ω·cm.

When the insulating dielectric layer of the electrostatic chuck according to the present invention is provided with grooves or depressions for dispersing a gas over the attracting face of the insulating dielectric layer as mentioned above, the gas can be uniformly dispersed or diffused in the gas-diffusing depression if the depth of depression is set at not less than 100 μm so that the temperature of a target object to be treated, such as a semiconductor wafer may be made uniform. As mentioned above, if the thickness of the insulating dielectric layer is more than 5.0 mm, the attracting force decreased. Therefore, the depth of the gas-diffusing depression is preferably not more than 5.0 mm.

The present invention can be embodied in an electrostatic chuck as shown in Fig. 1. An electrode 33 is formed on a substrate 31, and an insulating dielectric layer 32 is made upon the electrode 33. A gas-diffusing depression 34 is provided to be opened at a surface side of the insulating dielectric layer 32, and a gas-introducing hole 35 is communicated with the gas-diffusing depression 34. The gas-introducing hole 35 is opened at a surface side of the substrate 31, and connected to a gas feeder not shown. A gas is flown into the gas-diffusing depression 34 through the gas-introducing hole 35 as shown by an arrow E.

The depth t of the gas-diffusing depression 34 as measured from the attracting face is greater than that g of the electrode 33 from the attracting face, so that the electrode is buried in the substrate, while avoiding the location of the

The electrostatic chuck according to the present invention may be produced by the following process. First, a planar electrode made of a metallic bulky body is buried in a ceramic green body. This step is carried out as follows:

Method 1:

A preliminarily green body is prepared, and the above electrode is placed on this preliminarily green body. Then, a ceramic powder is charged over this electrode on the preliminarily green body, and the resultant is uniaxially press molded.

Method 2:

Two planar green bodies are prepared by cold isostatic press, and an electrode is held between two planar green bodies. Then, the assembly of the two green bodies and the electrode is hot pressed in this state.

In the method 2, the density of the preliminarily green body is increased and the variation in density of the green body is smaller owing to the cold isostatic press, as compared with the method 1. Therefore, as compared with the method 1, a shrinkage amount of the green body during the hot press is smaller and variation in density is smaller after the firing. As a result, the average dielectric strength of the sintered body is relatively larger.

The above function and effect is particularly important for the electrostatic chuck. For, due to the above-mentioned reasons, the average dielectric strength of the dielectric layer of the electrostatic chuck can be further enhanced, and its reliability can be greatly high.

In this sense, the relative density of the green body obtained by the cold isostatic press is most preferably not less than 60 %.

Further, in order to screen print an electrode on a surface of a green body obtained by the cold isostatic press process, the green body needs be dewaxed for a long time under a non-oxidizing atmosphere. In this respect, since such an extended time dewaxing step does not exist in a case where the electrode is held between the green bodies obtained by the cold isostatic press, this case is advantageous from the standpoint of the mass production.

Further, assume that the filmy electrode is formed by the screen printing. It is considered that since the filmy electrode is deformed during the hot pressing, another problem consequently occurs that the thickness of the dielectric layer on the electrode film becomes non-uniform. In this respect, since the deformation of the electrode can be prevented by the rigidity of the electrode itself during the hot pressing when the electrode made of a planar metallic bulky body is buried, the non-uniform thickness of the dielectric layer can be prevented. The thickness of the dielectric layer is important for the electrostatic chuck, because this thickness rules the chucking performance. The wording "planar metallic bulky body" used here means, for example, a metallic bulky body formed as a monolithic planar shape as shown in Figs. 3, 4 and 5 without forming a wire body or a planar body in a spiral or meandered or zigzag shape.

Since the electrode is subjected to hot press in its thickness direction, it is preferably a planar electrode from the standpoint of preventing the warping during the hot press. The electrode is preferably made of a high melting point metal in an application where the temperature is raised to a high temperature of 600°C or more at the maximum.

As such a high melting point metal, tantalum, tungsten, molybdenum, platinum, rhenium, hafnium and their alloys may be recited. From the standpoint of preventing contamination of the semiconductors, tantalum, tungsten, molybdenum, platinum and their alloys are preferred. As an object to be treated by using the electrostatic chuck, aluminum wafers may be recited by way of example in addition to the semiconductor wafers.

The configuration of the electrode includes a planar electrode having a number of small holes, and a net-shaped electrode besides the thin planar electrode. When the planar electrode having a number of the small holes or the net-shaped electrode is used as the electrode, the ceramic powder flows around through the numerous small holes or meshes, the joining force between the substrate and the insulating dielectric layer on the opposite sides of the electrode becomes greater to enhance the strength of the substrate. Further, when the electrode takes a thin planar shape, a large stress occurs particularly at the peripheral portion of the electrode, so that the substrate might be broken due to this stress. However, when the electrode is the planar body having numerous small holes or the net body, that stress is effectively dispersed by numerous small holes and meshes.

As the planar body having numerous small holes, a punched metal may be recited by way of example. However, when the electrode is to be made of a high melting point metal punched, such a high melting point metal itself has high hardness. Thus, it is difficult to punch numerous small holes in such a high melting point metal, and such punching raises a working cost.

In this respect, when the electrode is made of a metal net, wires made of the high melting point metal are easily available, and the metal net can be easily produced by knitting the wires. Therefore, the electrode can be easily produced by using such wires.

The mesh shape, the wire diameter, etc. of the metal net are not particularly limited. However, the metal nets having a wire diameter range of 0.03 mm to 0.5 mm and a mesh range of 150 meshes to 6 mesh could be used without

On operation of the electrostatic chuck, a gas is fed through the feed pipes 22 in an arrow B direction, passed through the gas-introducing holes 42, and blown out from their outlets on the attracting surface side in arrow C directions. The gas flows in the gas-diffusing depression 24A in an arrow D direction in a circular shape as viewed in plane, and also flows toward the projection 25 through the gas-diffusing depressions 24B in the arrow C directions. The gas is dispersed over the circular discoidal and trapezoidal-section portions 27, 29 excluding the round projections 26 so that the gas may be uniformly dispersed all over the rear face of the object to be treated.

The residual attracting force upon the object to be treated can be controlled by the design of the projections 26 so that the residual attracting force may not be excessive.

(Experiments)

In the following, more concrete experimental results will be explained.

(Experiment 1)

An electrostatic chuck as shown in Figs. 6 and 7 was produced. An electrode was buried in a green body composed of aluminum nitride powder having a purity of 99.9 %, and a sintered body was obtained by hot press sintering the green body at the hot press temperature of 1910°C, so that the volume resistivity of an insulating dielectric layer was controlled to 1×10^{11} Ω·cm at room temperature.

As an electrode, a metal net made of molybdenum was used. This metal net was obtained by knitting molybdenum wires having a diameter of 0.12 mm at a density of 50 wires per one inch. The surface of the insulating dielectric layer was machined to adjust the thickness thereof. A hole was formed in the sintered body from a rear face side by using a machining center, and a terminal was joined to the electrode. The relative density of the aluminum nitride sintered body constituting the substrate and the insulating dielectric layer was 99 %.

The average thickness of the insulating dielectric layer was varied as shown in Table 1. Each electrostatic chuck was placed in a vacuum chamber, and electric power was applied to a resistive heating element 19 in a controlled condition so that the temperature of the electrostatic chuck might be 200°C. The volume resistivity of the insulating dielectric layer at 200°C was 2×10^{8} Ω·cm. The attracting force was measured by the method explained with reference to Fig. 2. The voltage was 500 V or 1000 V. Results in the voltage of 500 V are given in Table 1, and those in the voltage 1000 V are shown in Table 2. The measurement values are given with respect to unit of 5 g/cm^2.

Table 1

Thickness of insulating dielectric layer (mm)	0.3	0.5	1.0	1.5	2.0
Attracting force (g/cm^2)	280	210	135	95	60
Thickness of insulating dielectric layer (mm)	3.0	4.0	5.0	6.0	-
Attracting force (g/cm^2)	45	35	30	5	-

Table 2

Thickness of insulating dielectric layer (mm)	0.3	0.5	1.0	1.5	2.0
Attracting force (g/cm^2)	395	360	180	155	105
Thickness of insulating dielectric layer (mm)	3.0	4.0	5.0	6.0	-
Attracting force (g/cm^2)	60	45	40	10	-

As is clear from the results, reduction in the attracting force is relatively small in the case of the insulating dielectric layer being in a thickness range of 0.5 to 5.0 mm, and preferably in a thickness range of 1.0 to 3.0 mm. In particular, a semiconductor could be sufficiently stably attracted in the case that the pressure of the gas was about 20 torr.

(Experiment 2)

An electrostatic chuck was produced in the same manner as in Experiment 1, and the attracting force was tested in the same way as in Experiment 1. In Experiment 2, the hot press temperature was set at 1800°C, and the volume resistivity of the insulating dielectric layer was controlled to 1×10^{15} Ω·cm at room temperature.

The electrostatic chuck was placed in a vacuum chamber, and was heated up to 400°C by feeding electric power

Table 4 (continued)

Surface roughness, Rmax, of insulating dielectric layer (μm)	Porosity of insulating dielectric layer (%)	maximum Pore diameter of insulating dielectric layer (μm)	Voltage applied to insulating dielectric layer (V)	Attracting force of electrostatic chuck (g/cm^2)
4	0.1	0.5	750	60
3	0.1	0.5	250	100
3	0.1	0.5	500	170
3	0.1	0.5	750	230
1	0.1	0.5	250	210
1	0.1	0.5	500	470
1	0.1	0.5	750	720

Table 5

Surface roughness, Rmax, of insulating dielectric layer (μm)	Porosity of insulating dielectric layer (%)	Maximum pore diameter of insulating dielectric layer (μm)	Voltage applied to insulating dielectric layer (V)	Attracting force of electrostatic chuck (g/cm^2)
3	3	1	250	95
3	3	1	500	160
3	3	1	750	210
3	5	2	250	40
3	5	2	500	60
3	5	2	750	95

As is clear from the above results, if the surface roughness, Rmax, of the insulating dielectric layer is not less than 4 μm, the attracting force is not almost increased even if the voltage applied to the insulating dielectric layer is raised, whereas if the surface roughness, Rmax, is not more than 3 μm, the attracting force is not only increased but also the attracting force sharply varies to respond to the increase in the voltage applied to the insulating dielectric layer. Further, it was also clarified that if the surface roughness, Rmax, is set at not more than 3 μm and if the porosity is set at not more than 3 %, the attracting force is most enhanced. Examination of various maching conditions revealed that if the maximum pore diameter of the insulating dielectric layer is not more than 5 μm, the surface roughness, Rmax, can be controlled to 3 μm.

(Experiment 4)

An electrostatic chuck as shown in Figs. 6 and 7 was produced. Aluminum nitride powder containing yttria as a sintering aid and having a purity of 95 % was used. An electrode was buried in a green body composed of this powder, and a sintered body was produced by hot press sintering the green body. As the electrode, a metal net made of molybdenum was used. A metal net obtained by knitting molybdenum wires having diameter of 0.3 mm at a density of 20 wires per inch was used. A molybdenum wire was buried as a resistive heating element. The surface of an insulating dielectric layer was machined to set its thickness at 3.0 mm. A hole was formed from a rear face side by using a machining center, and a terminal was joined to the electrode.

Round projections 26, a circular portion and trapezoidal-section portions were formed by sand blasting such that the height of the projections 26 from the circular portion or the trapezoidal-section portions were 20 μm. Each of gas-diffusing depressions was 3.0 mm in width and 1.0 mm in depth. The distance between the bottom face of the gas-diffusing depression and the electrode was 2.0 mm.

The relative density of the aluminum nitride sintered body constituting the substrate and the insulating dielectric layer was 99.9 %. In this case, if the dielectric breakdown resistance is at least 10 kV/mm and the distance between the bottom face of the gas-diffusing depression and the electrode is 500 μm, the dielectric breakage resistance is not

FIG. 1

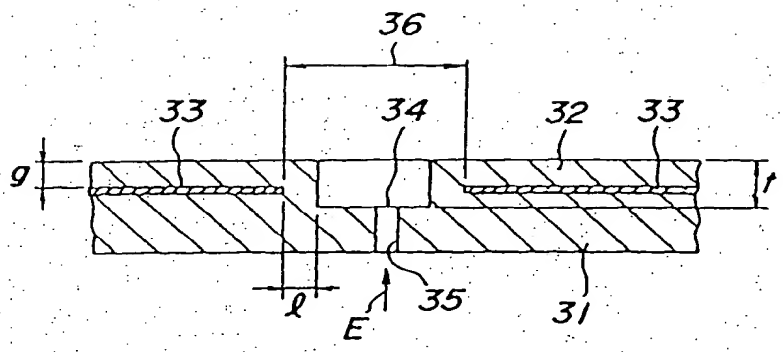


FIG_3

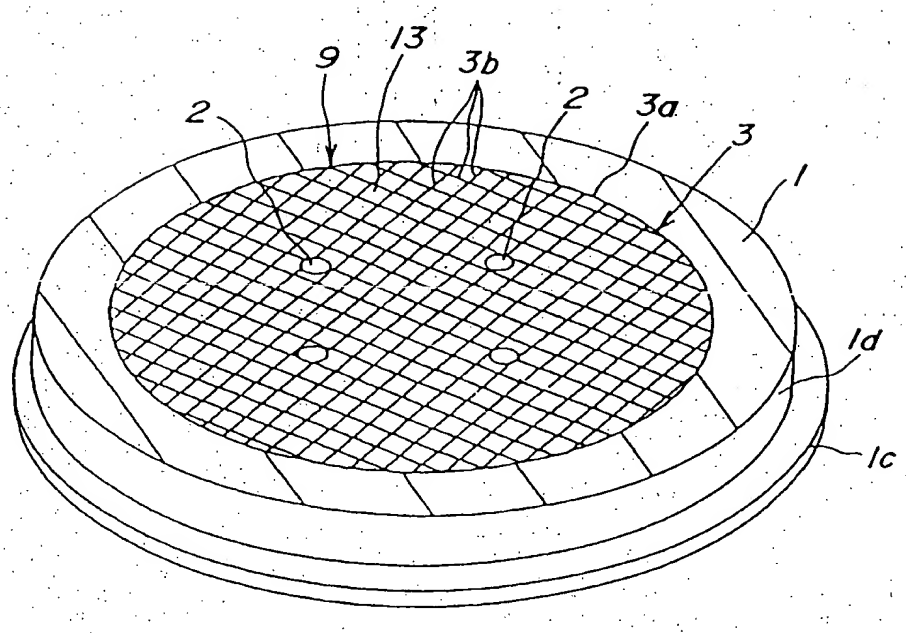


FIG_4

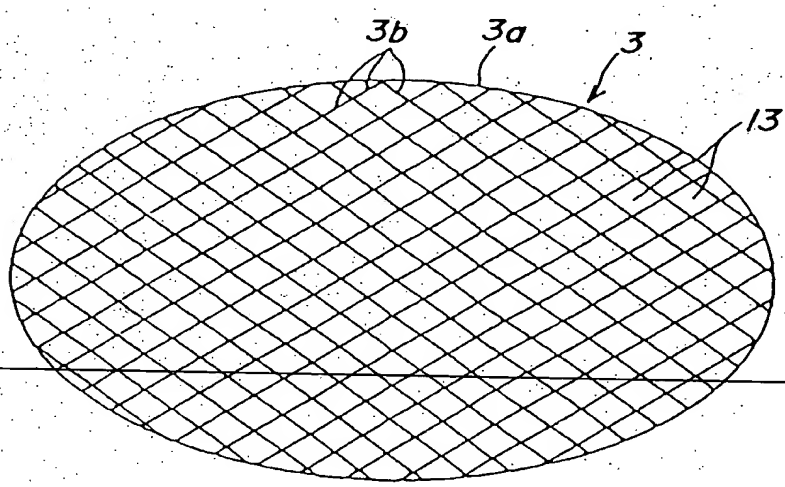
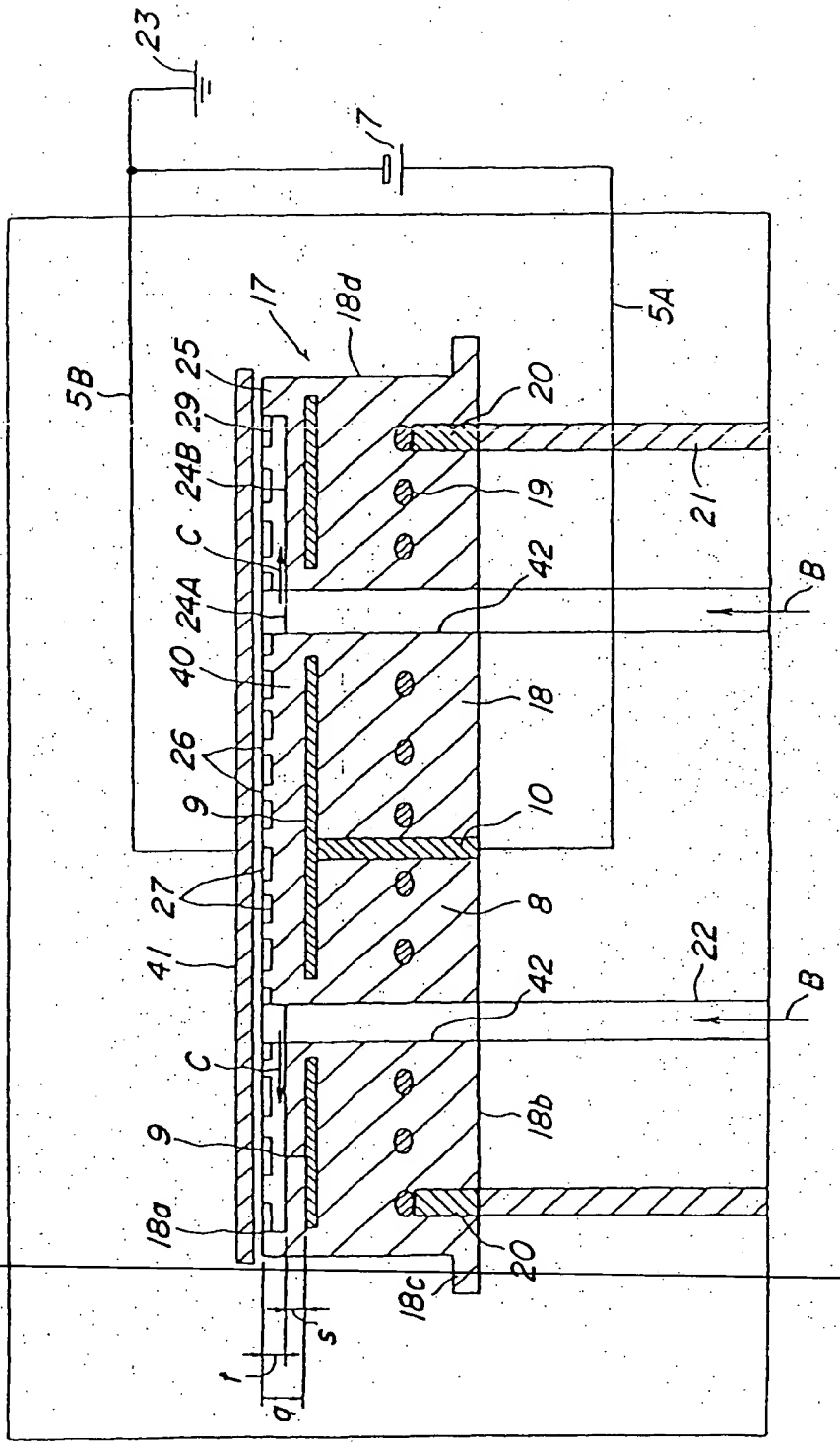


FIG. 6


23
17
5B
54
17
18d
25
29
24B
C
24A
40
26
9
27
41
C
9
18a
20
19
42
18
10
8
42
18b
20
18c
21
B
22
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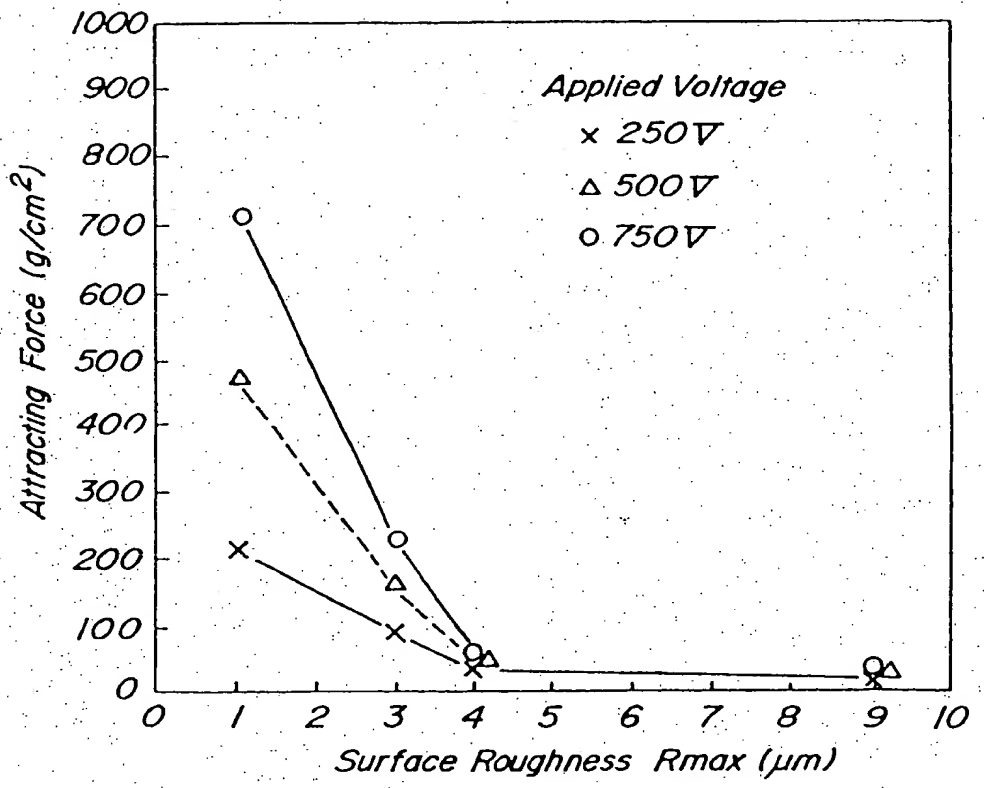
s
t
q

FIG_8


Attracting Force (g/cm²)
1000
900
800
700
600
500
400
300
200
100
0
0 1 2 3 4 5 6 7 8 9 10
Surface Roughness Rmax (μm)
Applied Voltage
× 250V
△ 500V
○ 750V

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 791 956 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
05.11.1997 Bulletin 1997/45

(43) Date of publication A2:
27.08.1997 Bulletin 1997/35

(21) Application number: 96306414.2

(22) Date of filing: 04.09.1996

(51) Int Cl.6: H01L 21/68, H01L 21/00

(84) Designated Contracting States:
DE FR GB

(30) Priority: 06.09.1995 JP 229190/95
20.08.1996 JP 218259/96

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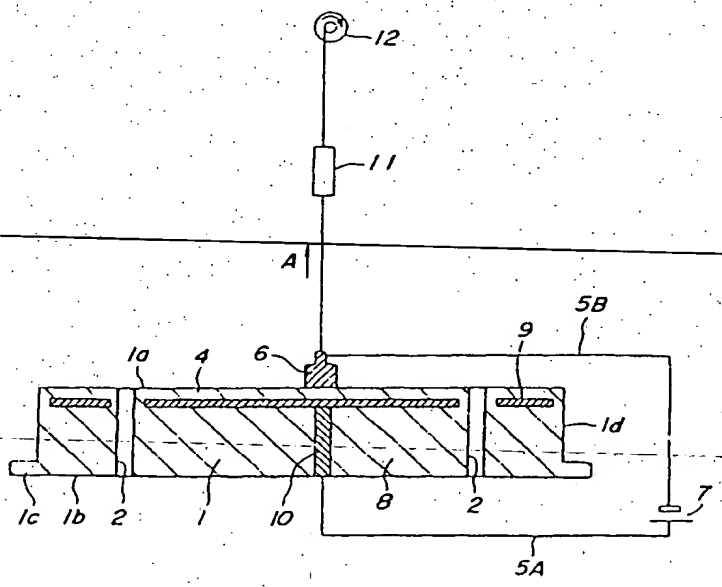
(54) Electrostatic chuck

(57) An electrostatic chuck for attracting an object to be treated, includes a substrate(1), an insulating dielectric layer (4) and at least one electrode (9) provided between the substrate and the insulating dielectric layer, wherein the above object is to be attracted onto the electrode via the insulating dielectric layer and an average thickness of the insulating dielectric layer (4) is not less than 0.5 mm and not more than 5.0 mm.

FIG_2



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EP 96 306 414

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

See Sheet B.

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

EP 96 306 414.2 - B -

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-5, 9 : Electrostatic chuck wherein the insulating dielectric has a thickness in the range 0.5-5.0mm.

2. Claims 6, 7, 8 : Electrostatic chuck having a gas-introducing hole and a gas-diffusing depression formed in the insulating dielectric layer and having a depth in the range 100μm to 5.0mm.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 790 641 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
20.08.1997 Bulletin 1997/34

(51) Int.Cl.[6]: H01L 21/00

(21) Application number: 97200338.8

(22) Date of filing: 07.02.1997

(84) Designated Contracting States:
CH DE FR GB IT LI NL

(30) Priority: 16.02.1996 US 602432

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(54) Wafer cooling device

(57) A wafer cooling device (WCD) for cooling a substrate, such as a wafer, during processing is presented. The substrate is mounted to an WCD heat transfer surface, thereby forming a cavity in between the substrate and the heat transfer surface into which gas is incorporated. An array of protuberances within the cavity provide support for the wafer. Contact heat conduction between the substrate and WCD is reduced by reducing the amount of direct contact between the substrate and WCD. Thus the heat transfer coefficient from the substrate, and hence substrate temperature, is controlled by adjusting the gas pressure in the cavity. In alternative embodiments, gas distribution channels are formed in the WCD heat transfer surface to increase gas pressure uniformity between the wafer and the WCD thus improving temperature uniformity across the substrate.

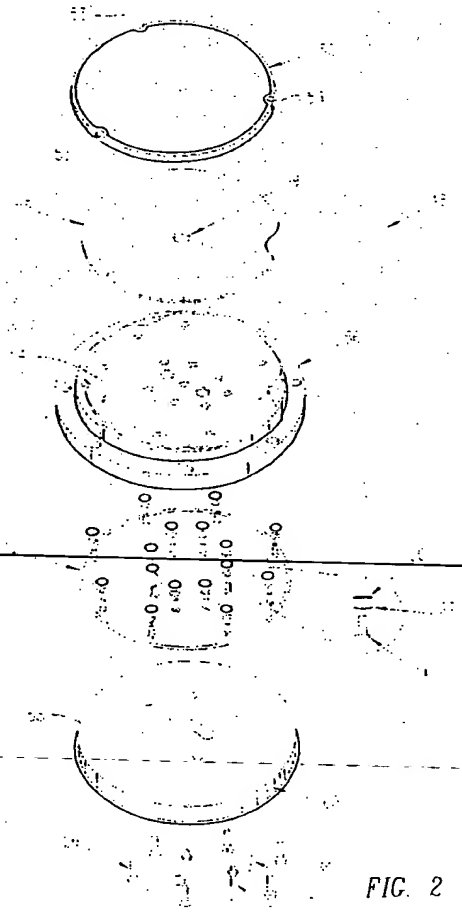

FIG. 2

EP 0 790 641 A1

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disk and the ceramic/cooling disk assembly is bolted into a cavity formed in the metallic support disk.

To reduce the area of contact between the WCD heat transfer surface and the wafer, a portion of the WCD heat transfer surface is recessed. The remaining WCD contact surface is roughened. This reduces heat conduction through direct contact between the wafer and the WCD. Thus the dominant heat transfer mechanism is through the gas between the wafer and the WCD wherein the gas pressure determines the heat transfer coefficient, hence wafer temperature. Gas distribution channels are formed in the WCD heat transfer surface to decrease gas pressure variations between the wafer and the WCD which result from gas leakage. Since the heat transfer coefficient, and wafer temperature, are mainly dependent on the gas pressure, providing a uniform gas pressure decreases temperature variations across the wafer.

In one embodiment, the gas distribution channels are arranged in a triangular pattern. In another embodiment, the gas distribution channels are arranged in a cross hatch pattern. In alternative embodiments, the gas distribution channels radiate outward in a spoke pattern from a central location on the WCD heat transfer surface. In another embodiment, eighteen gas distribution channels radiate outward from a hexagonal pattern of channels at the center of the WCD.

In all of the embodiments, one or more electrodes can be formed within the ceramic disk. A DC voltage is applied to the electrode(s) to produce electrostatic force which clamps the wafer to the WCD. In addition, RF power can be applied to the electrode(s) and also to the metallic support disk. For example, it may be desirable to apply RF power to accelerate ions towards a wafer mounted to the WCD, thus producing sputter etching of the wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a prior art electrostatic chuck.

Fig. 2 is an exploded top isometric view of a wafer cooling device (WCD) in accordance with the present invention.

Fig. 3 is a top isometric view of a metallic cooling disk in accordance with the present invention.

Fig. 4 is a cross sectional view of a unit into which the WCD in accordance with the present invention is installed.

Fig. 5 is a cross sectional view of a WCD in accordance with the present invention.

Fig. 6 shows a blown up cross sectional view of a portion of the wafer-WCD interface shown in Fig. 5.

Fig. 7 shows a hypothetical wafer-WCD assembly in which there is no direct contact between the surfaces of the wafer and the WCD.

Fig. 8 is a graph which shows the temperature profile along the heat transfer path from the wafer through the WCD.

Fig. 9 is a graph which illustrates the behavior of the heat transfer coefficient in relation to gas pressure and contact surface spacing.

Fig. 10a shows a top view of the contact surface of the ceramic disk for a WCD in accordance with the present invention.

Fig. 10b further illustrates the gas distribution channels for the WCD shown in Fig. 10a.

Figs. 11a and 11b are expanded top and cross sectional views, respectively, of a region of the ceramic disk shown in Fig. 10a.

Fig. 12 is a graph which shows the relation between the heat transfer coefficient and wafer surface roughness for various WCDs in accordance with the present invention.

Fig. 13 is a graph which shows the overall heat transfer coefficient versus gas pressure measured at the center of a WCD in accordance with the present invention.

Fig. 14 is a graph which illustrates the effects of pressure non-uniformity on wafer temperature for a WCD in accordance with the present invention.

Figs. 15a, 16a, 17a, 18 and 19a illustrate top views of WCDs with various configurations of gas distribution channels in accordance with alternative embodiments of the present invention.

Figs. 15b, 16b, 17b and 19b further illustrate the gas distribution channels for the embodiments shown in Figs. 15a, 16a, 17a, and 19a, respectively.

Fig. 20 is a graph which illustrates wafer temperature profiles for several WCDs in accordance with alternative embodiments of the present invention.

Fig. 21 is a graph which illustrates temperature versus backside gas pressure at the center of a WCD in accordance with the present invention.

Figs. 22a and 22b are exploded top isometric and cross sectional views of an alternative embodiment of the present invention in which the ceramic disk is brazed or soldered directly on to the metallic cooling disk.

Fig. 23 is a block diagram which illustrates means for controlling backside gas pressure of a WCD in accordance with the present invention.

across first thermally conductive paste layer 54, through metallic support disk 56, across second thermally conductive paste layer 58, and finally through metallic cooling disk 60. Heat (shown as Q_{out}) is removed from metallic cooling disk 60 by cooling water which contacts and cools metallic cooling disk 60, as discussed above in reference to Fig. 3.

Referring to Fig. 5, there are two primary pathways for heat transfer across wafer-WCD interface 50. The first is conduction through the gas in gap 68, hereinafter referred to a gas heat conduction. The second is conduction directly across the microscopic points of contact between contact surfaces 80, 82 at wafer-WCD interface 50, hereinafter referred to as contact heat conduction.

The two heat transfer pathways shall be discussed separately. First, gas heat conduction shall be discussed assuming that there is no contact heat conduction, i.e., that there is no direct contact between contact surfaces 80, 82. Fig. 7 shows a hypothetical wafer-WCD assembly in which there is no direct contact between contact surfaces 80, 82. Since there is no direct contact at wafer-WCD interface 50, there is no contact heat conduction. Thus all heat transfer across wafer-WCD interface 50 in Fig. 7 occurs across gap 68 through gas heat conduction.

The overall heat transfer coefficient h_0 for the wafer-WCD assembly illustrated in Fig. 7 can be calculated by first calculating the heat transfer coefficient across each layer in the heat transfer path. Calculated and measured heat transfer coefficients are given below in Table 1 where metallic support disk 56 is aluminum, metallic cooling disk 60 is brass, and gap 68 is filled with Helium at 10 Torr.

TABLE 1

Step	Heat Transfer Medium	Heat Transfer Coefficient for Step (W/M^2-K)
1	Wafer-WCD Interface 50 (with He at 10 Torr)	$h_1 = 275$
2	Ceramic Disk 52 (6.7 mm)	$h_2 = 2500$
3	Thermal Paste 54 (0.13 mm)	$h_3 = 18110$
4	Support Disk 56 (Aluminum at 6.35 mm)	$h_4 = 36220$
5	Thermal Paste 58 (0.13 mm)	$h_5 = 18110$
6	Cooling Disk (Brass at 3.18 mm)	$h_6 = 39370$
	Overall	$h_0 = 238$

The heat transfer coefficient for any particular layer (i) is set forth in the following equation:

$$Q_i = h_i * A_i * \Delta T_i \quad (1)$$

where Q_i is the heat conducted, h_i is the heat transfer coefficient, A_i is the area through which heat is conducted, and ΔT_i is the temperature difference over which the heat is conducted.

The overall heat transfer coefficient h_0 across all of the layers is the series sum of all of the layer heat transfer coefficients as set forth in the following equation:

$$h_0 = ((1/h_1)+(1/h_2)+(1/h_3)+(1/h_4)+(1/h_5)+(1/h_6))^{-1} \quad (2)$$

The area A_i through which heat is conducted is substantially the same for each step (i) along the heat transfer path. Also, at steady state where Q_{in} equals Q_{out}, the heat conducted (Q_i) is the same for each step along the heat transfer path. Thus $h_i * \Delta T_i$ will be the same for each step (i) along the heat transfer path. Consequently, large temperature drops occur across layers having low heat transfer coefficients and small temperature drops occur across layers having large heat transfer coefficients.

The temperature profile along the heat transfer path from wafer 62 to metallic cooling disk 60 is shown in Fig. 8 for an input heat Q_{in} value of 2000 watts. As shown in Fig. 8, T1 is the temperature at contact surface 80 of wafer 62, T2 is the temperature at contact surface 82 of ceramic disk 52, T3 is the temperature at the bottom of ceramic disk 52,

Pressure control valve 120 is manufactured by Unit Instruments, model #C11-55719, although any similar control valve can be used. Controller 128 is also manufactured by Unit Instruments, model #URS-20P, although any similar controller can be used. Manometer 124 is manufactured by Tylan General, model #CMLA-21506, although any similar manometer can be used.

A valve 134, such as a needle valve, allows a fixed amount of gas to flow to pump 136. This insures a steady state condition for pressure control valve 120. Valve 134 is set such that the gas flow rate through pressure control valve 120 is at or near the gas flow rate which is optimal for pressure control valve 120, thus improving tolerances in gas flow rate control, hence improving tolerances in backside pressure control.

To determine what pressure value (the set point) should be set into controller 128 to achieve a certain wafer temperature, a lookup table is used. For any given process, the lookup table is a correlation of measured wafer temperature in relation to set point pressure. To generate the lookup table, the set point pressure is set to a first value and the wafer temperature is measured. The set point pressure is then set to second value and the wafer temperature is again measured. This iterative process continues and a lookup table is completed.

Alternatively, the wafer temperature is measured directly, and the measured temperature is used to control gas pressure. The wafer temperature can be measured using infrared techniques, or by using embedded or contact thermocouples well known to those skilled in the art. The wafer temperature is detected by a temperature sensor 138 (Fig. 23). Temperature sensor 138 delivers a signal representing the wafer temperature to controller 128 which in turn instructs pressure control valve 120 which adjusts the backside gas pressure and maintains the desired wafer temperature. To illustrate, if the wafer temperature is greater than the desired wafer temperature, controller 128 increases the backside gas pressure by instructing pressure control valve 120 to let more gas into the backside feed line. This decreases the wafer temperature to the desired valve. Conversely, if the wafer temperature falls below a desired wafer temperature, controller 128 decreases the backside gas pressure by instructing pressure control valve 120 to reduce the amount of gas into the backside feed line. This increases the wafer temperature to the desired value.

As described above, in the hypothetical arrangement shown in Fig. 7, it was assumed that there is no contact heat conduction at wafer-WCD interface 50. However, under certain conditions contact heat conduction can be substantial. Referring back to Figs. 5 and 6, the amount of heat transferred by contact heat conduction is determined by the size of the area of direct contact between contact surfaces 80, 82. The greater the area of direct contact, the greater the heat transferred by contact heat conduction. The size of the area of direct contact is a function of the roughness, flatness and hardness of contact surfaces 80, 82, as well as the applied pressure between contact surfaces 80, 82. Since the characteristics of contact surface 80 vary from wafer to wafer, and since the characteristics of contact surface 82 can change over time, accurately controlling contact heat conductance is difficult.

Two techniques are used to reduce the area of direct contact between contact surfaces 80, 82. First, a large percentage of the surface area available for contact is removed. Fig. 10a shows a top view of contact surface 82 of ceramic disk 52 for a preferred embodiment in accordance with the present invention. Fig. 11a shows an expanded top view of region 76 in Fig. 10a. Fig. 11b shows a cross sectional view of region 76 along the line A - A' shown in Fig. 11a. As seen in Fig. 10a, contact surface 82 has a dot pattern.

Top and cross sectional views of five dots 72 are shown in Fig. 11a and 11b, respectively. As seen in Fig. 11b, each dot 72 represents a raised surface area 72' of contact surface 82, with each dot having a diameter D_D typically within a range of approximately 1.5 mm to 2.5 mm. Hence, a wafer (not shown) mounted to ceramic disk 52 will only contact ceramic disk 52 along the surface 72' of the raised dots 72. Thus a large percentage of the surface area of contact surface 82 available for contact heat conduction is removed. It is desirable to remove between approximately 80 to 98 percent of the surface area of contact surface 82 available for contact heat conduction. In the embodiment shown in Fig. 10a, approximately 80 percent of the total surface area of contact surface 82 is recessed with only approximately 10 percent of the total surface area remaining for contact heat conduction. Although in the top views shown in Figs. 10a and 11a dots 72 are circular, it should be understood that dots 72 can be in any shape, for example triangular or rectangular.

A second technique to reduce the amount of direct contact between contact surfaces 80, 82 is to roughen contact surface 82 of ceramic disk 52. By roughening contact surface 82, the number of microscopic points of contact between contact surfaces 80, 82 are reduced. This reduces the amount of direct contact between contact surfaces 80, 82, and hence contact heat conduction.

Fig. 12 is a graph which shows the behavior of the heat transfer coefficient for contact heat transfer versus wafer surface roughness (roughness of contact surface 80 of wafer 62) for various WCDs. The WCDs in curves A, B and C, D have contact surfaces (82) with roughnesses of 0.05 and 0.35 μm Ra, respectively, where μm Ra is the average deviation in microns from a hypothetical mean plane generally parallel to the contact surface. Furthermore, the contact surfaces (82) in the WCDs in curves B and D are similar to the contact surface 82 shown in Fig. 10a and have 90% of the total surface area of contact surface 82 recessed.

As shown by the curve labeled A in Fig. 12, contact heat conductance can become quite efficient with a heat transfer coefficient of approximately 2000 W/M^2-K if contact surfaces 80, 82 are polished to less than 0.05 μm Ra. In

shown in curve H. Acceptable wafer temperature profiles (maximum temperature across the wafer surface below 400°C) are obtained with backside gas pressure drops of less than 10 percent (10.0 Torr at center, 9.0 Torr at edge) as shown in curve I. Thus it is desirable to avoid variations in the backside gas pressure of more than ten percent.

Another advantage of having a substantially uniform backside gas pressure is that lower overall wafer temperatures are obtained. This is because as the variation in backside gas pressure decreases, the average pressure behind the wafer rises, as does the average heat transfer coefficient. Thus, the overall wafer temperature drops, even at the wafer center. To illustrate, the temperature at the wafer center in curve G (1% variation) is substantially cooler than the temperature at the wafer center in curve H (90% variation) even though the backside gas pressure at the wafer center equals the inlet pressure of 10 Torr in both examples.

As shown in curve G, even when backside gas pressure varies by only one percent, the wafer edge is at a slightly higher temperature than the wafer center. This is because the wafer overhangs the edge of the WCD slightly, by approximately 1.0 mm, to accommodate tolerances in the placement of the wafer on the WCD, and the portion that overhangs sees little or no cooling other than by heat conduction through the wafer itself.

To contain the gas, a continuous annular ring 78 formed at the periphery of ceramic disk 52 (see Figs. 10a, 11a and 11b) provides a seal between wafer 62 and ceramic disk 52. Referring to Fig. 11b, the raised surface area 78' of annular ring 78, and the raised surface areas 72' of dots 72 are substantially coplanar, with an average deviation of less than 0.1 mm from a hypothetical mean plane generally parallel to surfaces 72', 78'. Ideally, with a perfect seal and no gas movement, there would be no pressure variation behind the wafer. However, realistically there will be some gas leakage past annular ring 78.

As discussed above, the WCD and hence annular ring 78 has a slightly smaller diameter than the wafer to accommodate for wafer placement tolerances. If the wafer is misplaced such that a portion of annular ring 78 does not contact a portion of the wafer, then the seal formed by annular ring 78 and the wafer is breached. When the seal is breached, the leak rate increases abruptly.

Even when the seal is not breached due to wafer misplacement, the seal will still leak. For a given leak rate q at the seal formed by the wafer 62 and the annular ring 78, the pressure distribution will be governed by the seal conductance C_S as set forth in the following equation:

$$q = C_S * \Delta P \qquad (3)$$

where ΔP is the pressure drop across the seal.

The seal conductance (C_S) depends upon several factors. One factor is the roughness of the contact surfaces that create the seal, i.e. the roughness of the surface of annular ring 78 and the roughness of the surface of the wafer 62 which contacts annular ring 78. Another factor is the presence of hard particles on the contact surfaces that create the seal. The magnitude of the clamping force between the contact surfaces that create the seal also effects the seal conductance. Since these factors are difficult to predict, the seal conductance is also difficult to predict. However, some control over the seal conductance can be obtained by increasing the width (shown as W_S in Figs. 11a and 11b) of annular ring 78, with larger widths producing smaller seal conductances and hence smaller leak rates.

For any given seal conductance, the maximum seal leak rate occurs when the pressure drop across the seal equals the maximum possible pressure drop according to equation 3. The maximum possible pressure drop is the difference between the backside gas inlet pressure (the pressure cannot exceed the backside gas inlet pressure) and the pressure in the vacuum chamber which for a 5 mTorr operating pressure is essentially zero for the purposes of these calculations. To limit variations in the backside gas pressure, the surface (82) pattern of ceramic disk 52 must permit flow rates in excess of the maximum seal leak rate. This occurs when the inner surface conductance (the gas flow conductance from the center of ceramic disk 52 to annular ring 78 in the gap formed by the wafer and ceramic disk 52) is much greater than the seal conductance.

The inner surface conductance depends upon the dot height H_D, since this sets the spacing through which gas flows. In WCDs having a greater dot height H_D the inner surface conductance is improved. However, as discussed previously, it is desirable to keep the dot height H_D below 40 µm to prevent heat transfer performance from degrading.

To improve inner surface conductance, gas distribution channels (shown as 74, 74' in Figs. 10a, 10b, 11a and 11b) are used. As shown in Fig. 10b, 18 gas distribution channels 74 radiate outward from a hexagonal pattern of channels at the center of the WCD. To insure that there are sufficient dots 72 at the center of ceramic disk 52, only six gas distribution channels are used inside of the hexagonal pattern to distribute gas from the central gas inlet port. The gas distribution channels supply gas to annular ring 78 to replace gas which leaks across the seal formed by annular ring 78 and the wafer, and to the vacuum chamber. Referring to Fig. 11b, gas distribution channels 74, 74' are rectangular in cross section and have a depth D_C and a width W_C. In one embodiment, the width W_C of gas distribution channels 74, 74' is approximately 1500 µm, and the depth D_C is approximately 700 µm. It is desirable that the width W_C of gas

TABLE 2 (continued)

Embodiment	Embodiment according to	Seal Width	Channel depth	Wafer Edge Pressure	Seal Leak Rate	Inner Surface Flow
		(mm)	(μm)	(Torr)	(SCCM)	(SCCM)
12	Fig. 18	2	300	4.3	6.5	1.10
13	Fig. 18	4	700	6.0	4.5	1.10
14	Fig. 18	2	700	9.1	13.5	14.50

In all of the embodiments shown in Table 2, the channel width was 1500 μm. The wafer edge pressure is the backside gas pressure at the inner edge of annular ring 78. The seal leak rate is the expected leak rate at the seal formed by the wafer and annular ring 78 for the corresponding wafer edge pressure shown in Table 2. The inner surface flow is the expected flow across the ceramic disk surface 82 when the backside gas pressure is 10.0 Torr at the wafer center and 9.0 Torr at the wafer edge (10% variation in backside gas pressure).

As shown in Table 2, in Embodiment 1 (Fig. 19a), the pressure varies 0.3 Torr across the inner surface from the inlet pressure of 10 Torr at the wafer center to 9.7 Torr at the wafer edge. Thus, in Embodiment 1, the backside gas pressure variation is 3%. Similarly, in Embodiments 5, 10, 11 and 14 the backside gas pressure variation is 3%, 5%, 3% and 9%, respectively. In Embodiment 1, the inner surface flow rate across the ceramic disk surface 82 is 50.00 SCCM (for a 1 Torr pressure drop between the wafer center and edge), which far exceeds the expected seal leak rate of 14.6 SCCM. This provides a measure of tolerance to accommodate higher seal leak rates which may result, for example, from wafer misalignment or particulate. Similarly, in Embodiments 5, 10 and 11, the inner surface flow rate of 50.00, 26.00 and 26.00 SCCM across the ceramic disk surface 52 substantially exceeds the expected maximum seal leak rate of 14.6, 14.2 and 7.3 SCCM, respectively, thus also providing a measure of tolerance to accommodate higher seal leak rates.

Expected heat transfer coefficients for Embodiments 1, 2, 5, 9 and 10 in Table 2 are given below in Table 3. Heat transfer coefficients given are for gas heat conduction only. In all of the embodiments, the heat transfer coefficient for contact heat conduction is within the range of approximately 5 to 30 W/M^2-K depending upon the wafer surface roughness, with rougher wafer surfaces resulting in lower heat transfer coefficients.

TABLE 3

Embodiment	% Variation	Heat Transfer Coefficient, Wafer Center (W/M^2-K)	Heat Transfer Coefficient, Wafer Edge (W/M^2-K)
1	3%	297	255
2	82%	223	89
5	3%	297	255
9	27%	279	204
10	5%	295	243

Table 3 illustrates that embodiments with less variation in backside gas pressure have less variation in the heat transfer coefficients between the wafer center and edge. For example, in Embodiment 1, which has a backside gas pressure variation of 3%, the heat transfer coefficients at the wafer center and edge are 297 and 255 W/M^2-K, respectively, for a variation of 42 W/M^2-K. However, in Embodiment 2, which has a much greater backside gas pressure variation of 82%, the heat transfer coefficients at the wafer center and edge are 223 and 89 W/M^2-K, respectively, for a variation of 134 W/M^2-K. Less variation in the heat transfer coefficient improves the wafer temperature profile as illustrated in Fig. 20.

In Fig 20, wafer temperature profiles for Embodiments 1 and 9 are shown in curves J and K, respectively, assuming a rough wafer surface (heat transfer coefficient for contact heat conduction equal to approximately 5 W/M^2-K). Wafer temperature profiles for Embodiment 2 with a smooth wafer surface and with a rough wafer surface area are shown in curves L and M, respectively. The heat transfer coefficients for contact heat conduction are 500, 30 W/M^2-K for curves L and M, respectively. Fig. 20 assumes a heat load of 2000 watts delivered to a 200 mm diameter wafer. The backside gas, helium, was supplied at 10 Torr through a centrally located gas feed. Ceramic disk 52 was held at 60°C.

As shown in curve M, wafer edge temperatures in excess of 700°C are obtained in Embodiment 2 with a wafer having a rough surface. However, as shown in curve L, when the wafer surface is polished a substantially uniform

contact plate and said cooling plate.

3. The substrate cooling device of Claim 2 wherein said support plate is interposed between said substrate contact plate and said cooling plate.

4. The substrate cooling device of Claim 3 further comprising:

a first layer of thermally conductive paste between a backside of said substrate contact plate and a first surface of said support plate; and

a second layer of thermally conductive paste between a second surface of said support plate and said cooling plate.

5. The substrate cooling device of Claim 4 further comprising a first seal for protecting said first layer of thermally conductive paste from a vacuum environment surrounding said substrate cooling device.

6. The substrate cooling device of Claim 5 further comprising a second seal for protecting said first layer of thermally conductive paste from a vacuum environment within said at least one gas inlet channel.

7. The substrate cooling device of Claim 3 further comprising a plurality of bolts for attaching said support plate to said substrate contact plate.

8. The substrate cooling device of Claim 7 wherein a belleville spring washer is used with each of said bolts to provide flexibility and thereby accommodate a difference between the respective thermal expansion properties of said support plate and said substrate contact plate.

9. The substrate cooling device of Claim 4 wherein said substrate contact plate is formed of a ceramic material.

10. The substrate cooling device of Claim 2 wherein said cooling plate is interposed between said substrate contact plate and said support plate.

11. The substrate cooling device of Claim 10 wherein said substrate contact plate is soldered or brazed to said cooling plate.

12. The substrate cooling device of Claim 1 wherein an area of said recessed region occupies from 80% to 98% of an area of said central region.

13. The substrate cooling device of Claim 1 wherein said peripheral raised region comprises an annular seal ring.

14. The substrate cooling device of Claim 13 wherein said at least one gas inlet channel opens into said cavity at a gas inlet port located at or near a center of said central region.

15. The substrate cooling device of Claim 13 further comprising an annular gas distribution ring located adjacent an inside edge of said annular seal ring.

16. The substrate cooling device of Claim 15 wherein said central region further comprises a pattern of gas distribution channels extending from said at least one gas inlet port to said annular gas distribution ring.

17. The substrate cooling device of Claim 16 wherein said gas distribution channels have a depth in the range of 0.2-2.0 mm and a width in the range of 0.5-2.5 mm.

18. The substrate cooling device of Claim 17 wherein said gas distribution channels have a depth of approximately 0.7 mm and a width of approximately 1.5 mm.

19. The substrate cooling device of Claim 16 wherein said pattern comprises an intermediate channel in the shape of a closed figure surrounding said at least one gas inlet port, a first group of channels extending from said gas inlet port to said intermediate channel, and a second group of channels extending from said intermediate channel to said annular gas distribution ring, said second group of channels being greater in number than said first group of

contact plate, a surface of said substrate being in contact with said raised region and said contact surfaces, a gas being introduced into said cavity through said at least one gas inlet channel.

40. The combination of Claim 39 wherein said gas is selected from the group which consists of hydrogen, helium, nitrogen and argon.

41. The combination of Claim 39 wherein a pressure of said gas in said cavity is at or below approximately 20 Torr.

42. The combination of Claim 39 wherein said substrate receives power from a source external to said substrate cooling device, a temperature of said substrate being controlled by said gas pressure.

43. The combination of Claim 42 wherein less than approximately 20% of said heat removed from said substrate is removed through said protuberances.

44. The combination of Claim 39 wherein a roughness of said surface of said peripheral raised region and said contact surfaces are greater than or equal to a roughness of a surface of said substrate in contact with said substrate cooling device.

45. The combination of Claim 39 further comprising:

a pressure control valve for controlling a pressure of a gas in said at least one gas inlet channel;
a pressure sensor for sensing a pressure of said gas in said at least one gas inlet channel;
a controller linked to said pressure control valve and said pressure sensor;
wherein said controller receives a signal from said pressure sensor and responsive thereto delivers a signal to said pressure control valve to maintain a the pressure in said at least one gas inlet channel at a predetermined level.

46. The combination of Claim 39 further comprising:

a pressure control valve for controlling a pressure of a gas in said at least one gas inlet channel;
a temperature sensor for sensing a temperature of said substrate;
a controller linked to said pressure control valve and said temperature sensor;
wherein said controller receives a signal from said temperature sensor and responsive thereto delivers a signal to said pressure control valve to maintain a temperature of said substrate at a predetermined level.

47. A chemical vapor reaction system comprising a reaction chamber and a wafer cooling device according to Claim 1, said wafer cooling device being positioned to support a wafer in said reaction chamber.

48. The chemical vapor reaction system of Claim 47 wherein said chemical vapor reaction system comprises a chemical vapor deposition system.

49. The chemical vapor reaction system of Claim 47 wherein said chemical vapor reaction system comprises a plasma-enhanced chemical vapor deposition system.

50. The chemical vapor reaction system of Claim 47 wherein said chemical vapor reaction system comprises a plasma etch system.

51. The chemical vapor reaction system of Claim 47 wherein said chemical vapor reaction system comprises a sputter etch system.

52. The chemical vapor reaction system of Claim 47 wherein said chemical vapor reaction system comprises a physical vapor deposition system.

53. A wafer cooling device comprising:

a ceramic disk, said ceramic disk having a top surface which comprises a raised annular ring extending along the periphery thereof and a central region inside said raised annular ring, said central region comprising a recessed area and an array of dots, each of said dots terminating in a contact surface, a surface of said raised

disk.

66. The wafer cooling device of Claim 65 wherein said cooling disk is fixed in said cavity with bolts.

67. The wafer cooling device of Claim 66 further comprising a first O-ring for sealing said cavity against a vacuum environment surrounding said wafer cooling device and a second O-ring for sealing said cavity against a vacuum environment in said gas inlet channel.

68. A method of controlling the temperature of a substrate which is receiving thermal energy from an external source, said method comprising the steps of:

providing a substrate cooling device which comprises a substrate contact plate having an annular raised ring formed at the periphery thereof and a cavity inside said annular raised ring;
clamping said substrate to a surface of said annular raised ring;
supplying a gas to said cavity;
establishing the pressure of the gas within said cavity so as to predetermine a temperature difference between said substrate and said substrate contact plate and thereby control the temperature of said substrate.

69. The method of Claim 68 further comprising the step of cooling said substrate contact plate.

70. The method of Claim 68 wherein a leakage of said gas flows between said substrate and said surface of said annular raised ring.

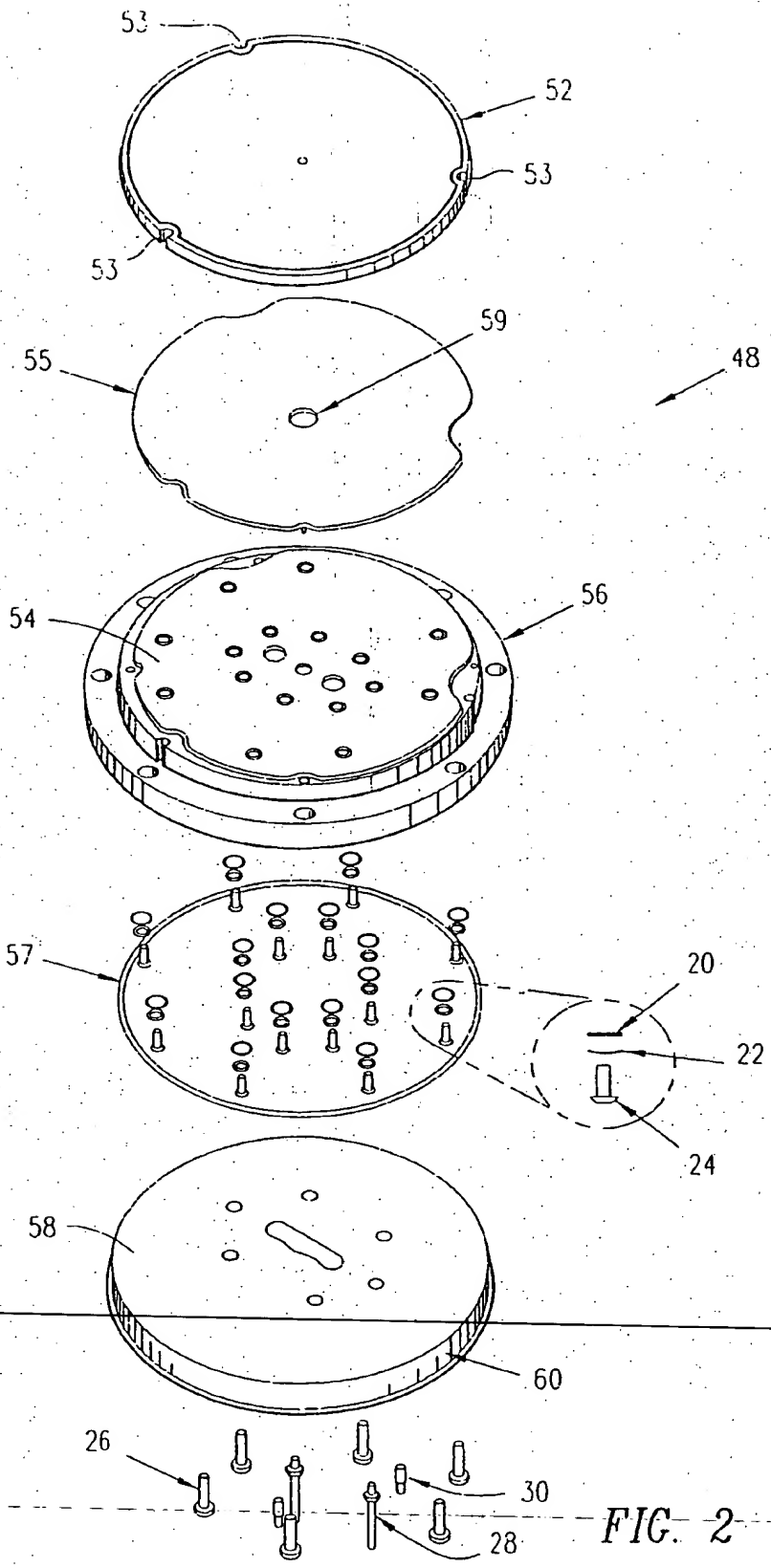

FIG. 2

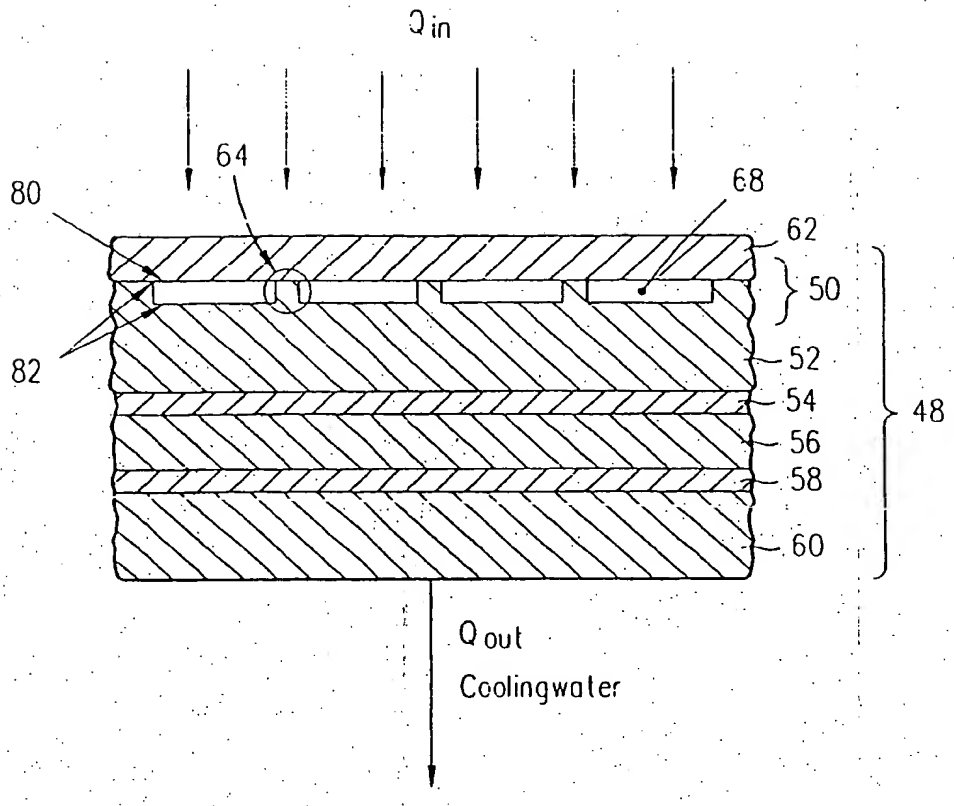
Q in
64
80
68
62
50
82
52
54
48
56
58
60
Q out
Coolingwater

FIG. 5

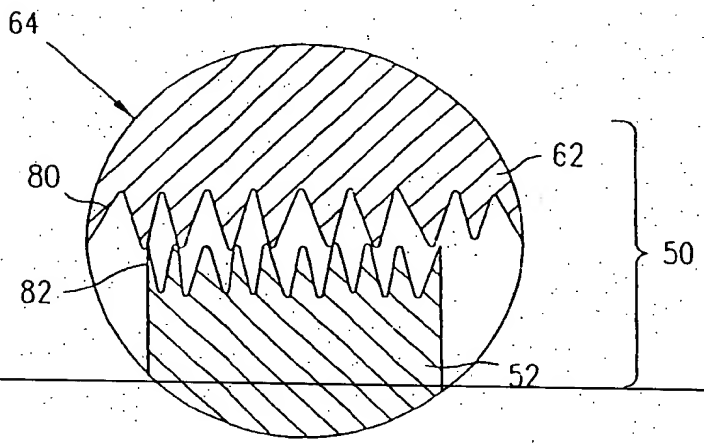
64
80
62
50
82
52

FIG. 6

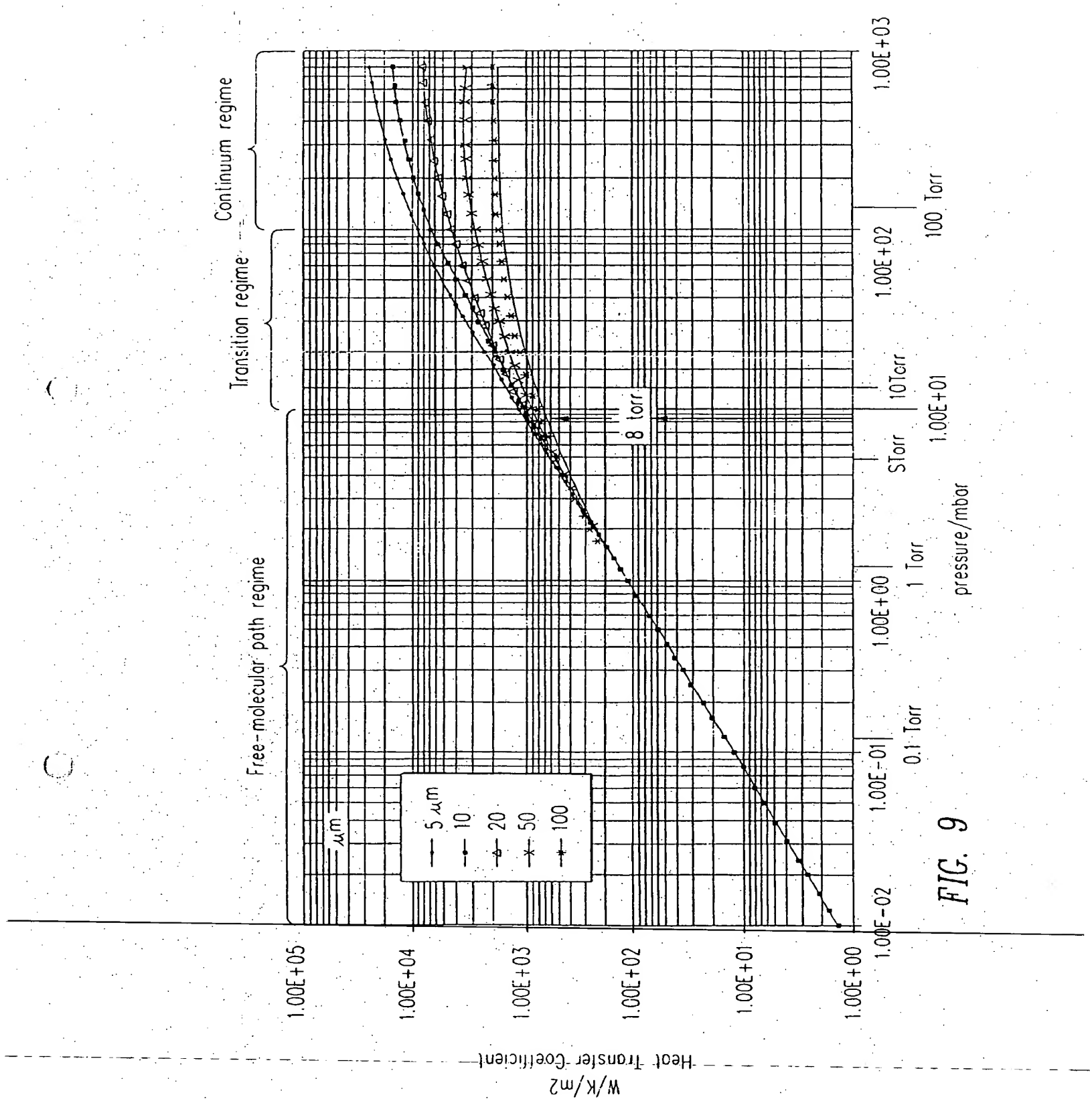
Heat Transfer Coefficient
W/K/m2
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
1.00E-02
1.00E-01
1.00E+00
1.00E+01
1.00E+02
1.00E+03
0.1 Torr
1 Torr
5Torr
10Torr
100 Torr
pressure/mbar
8 torr
Free-molecular path regime
Transition regime
Continuum regime
μm
5 μm
10
20
50
100

FIG. 9

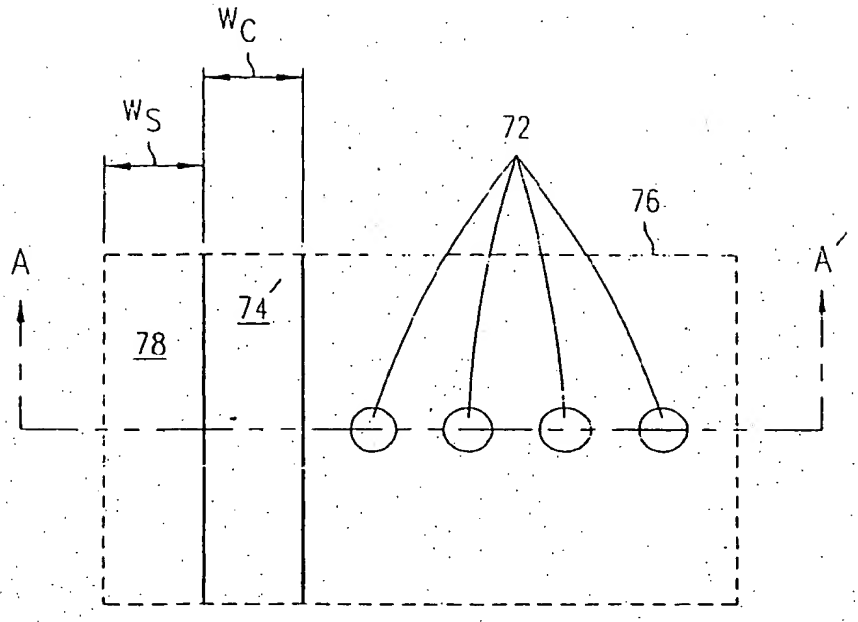

FIG. 11a

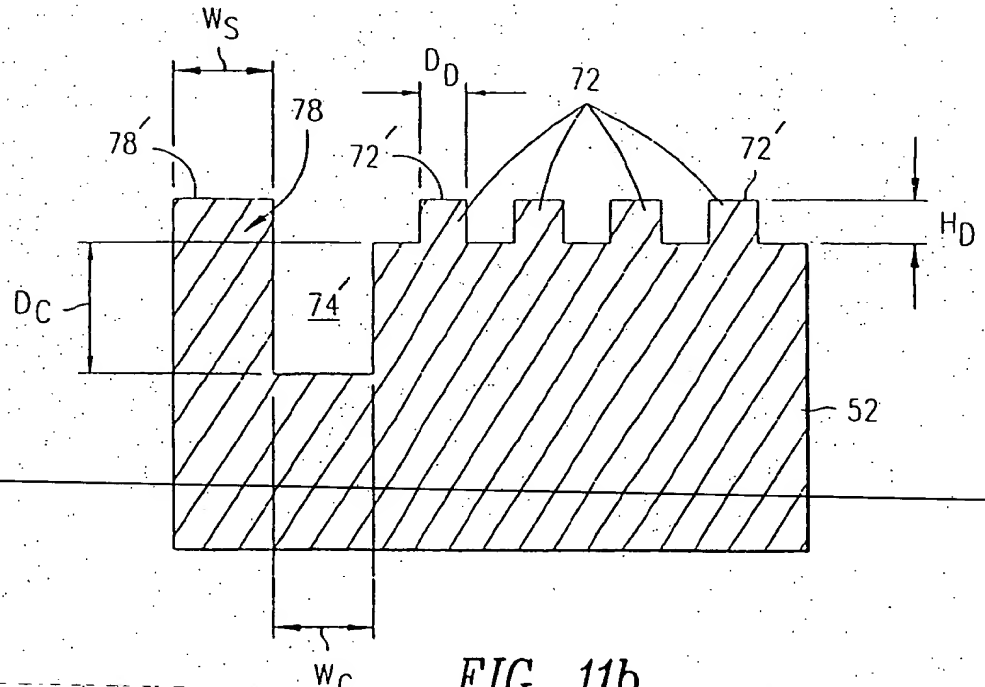

FIG. 11b

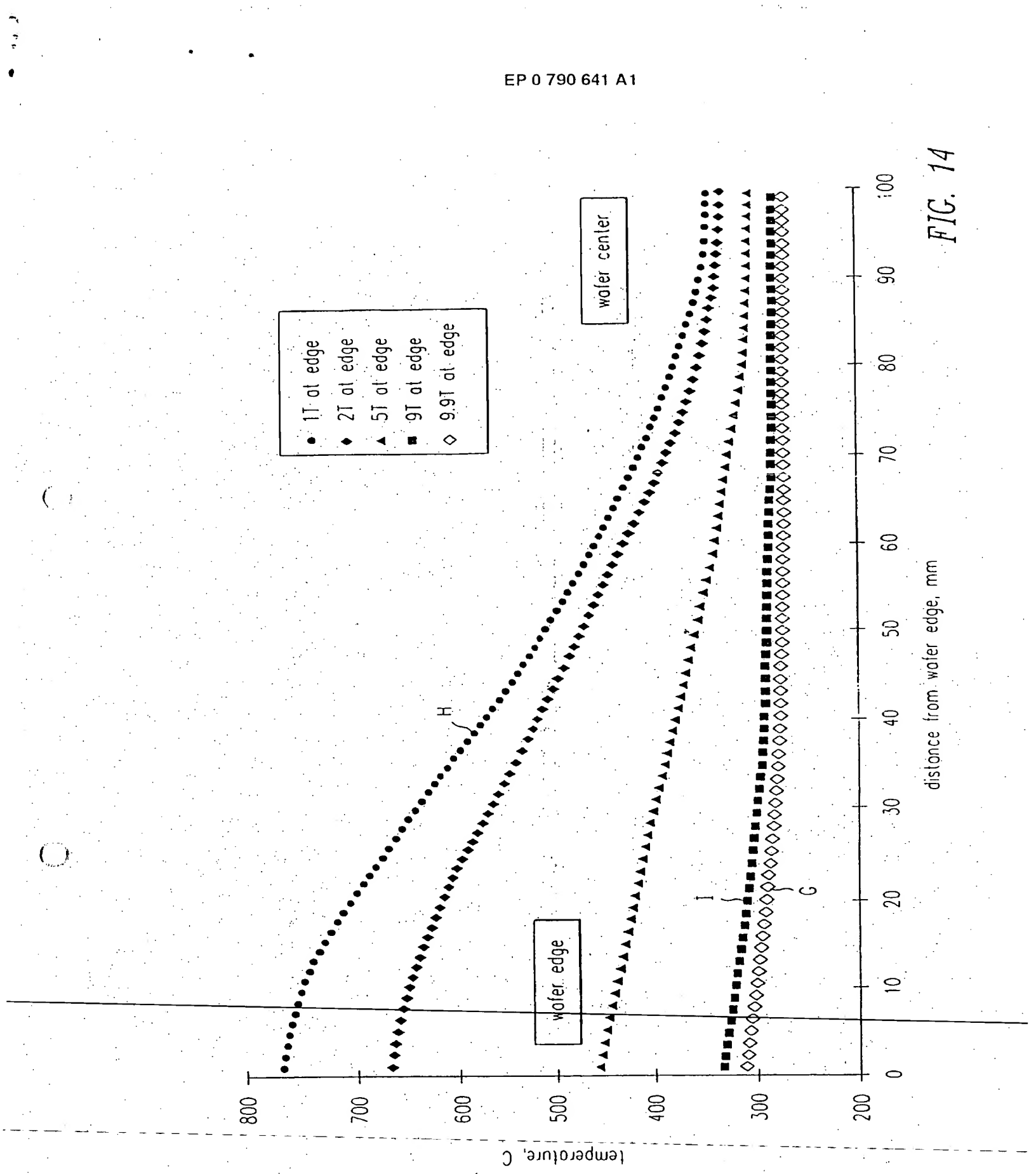
1T at edge
2T at edge
5T at edge
9T at edge
9.9T at edge
wafer center
wafer edge
H
I
G
temperature, C
distance from wafer edge, mm
800
700
600
500
400
300
200
0
10
20
30
40
50
60
70
80
90
100

FIG. 14

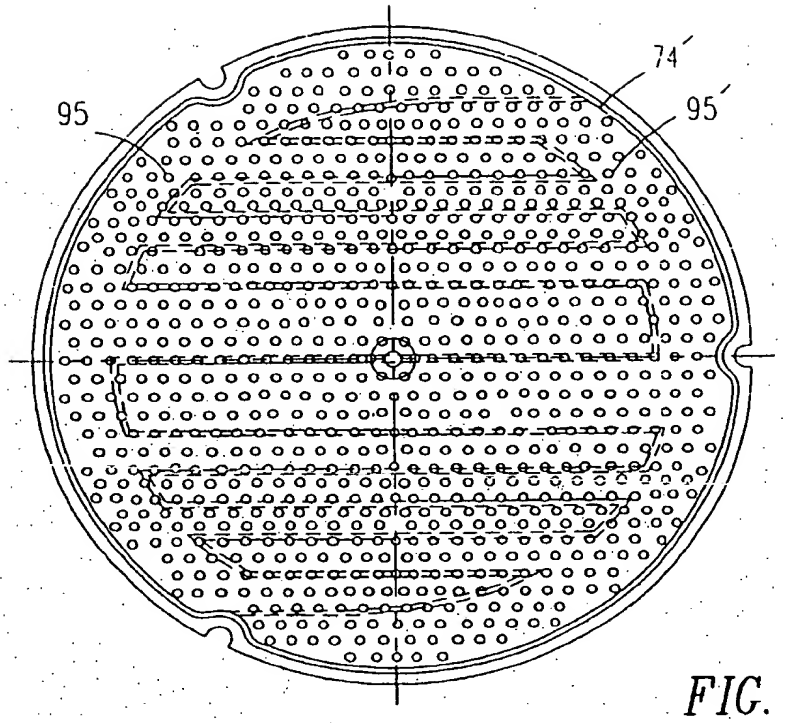

FIG. 16a

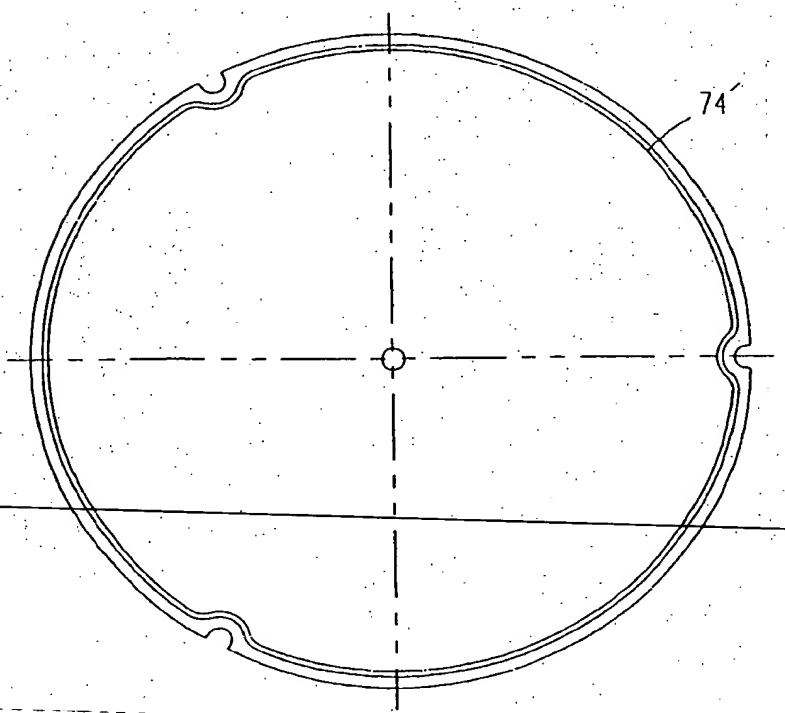

FIG. 16b

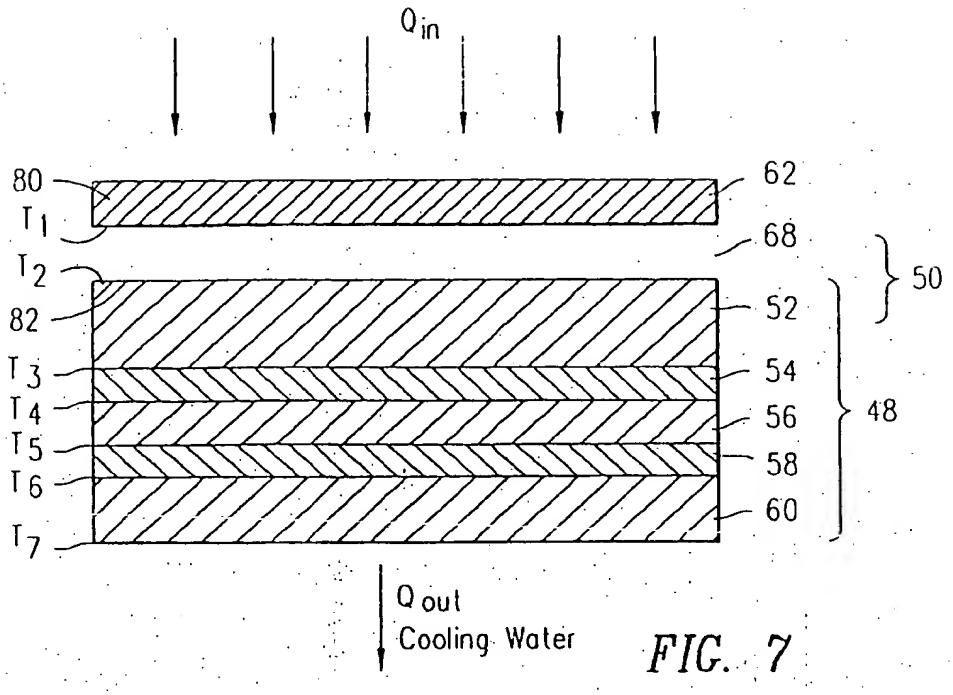
Q in
80
T1
62
68
T2
82
50
52
T3
54
T4
56
48
T5
58
T6
60
T7
Q out
Cooling Water

FIG. 7

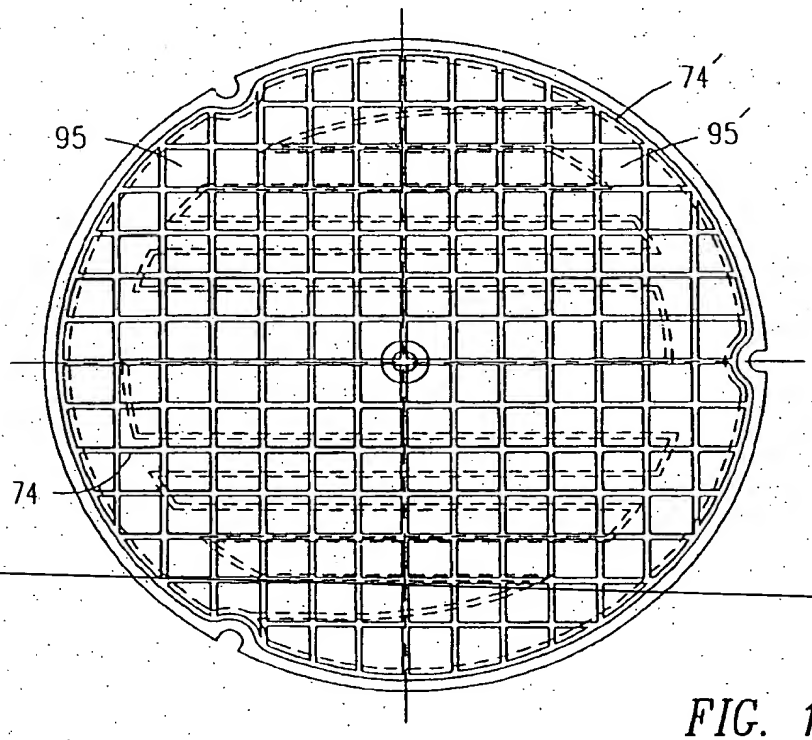
74'
95
95'
74

FIG. 18

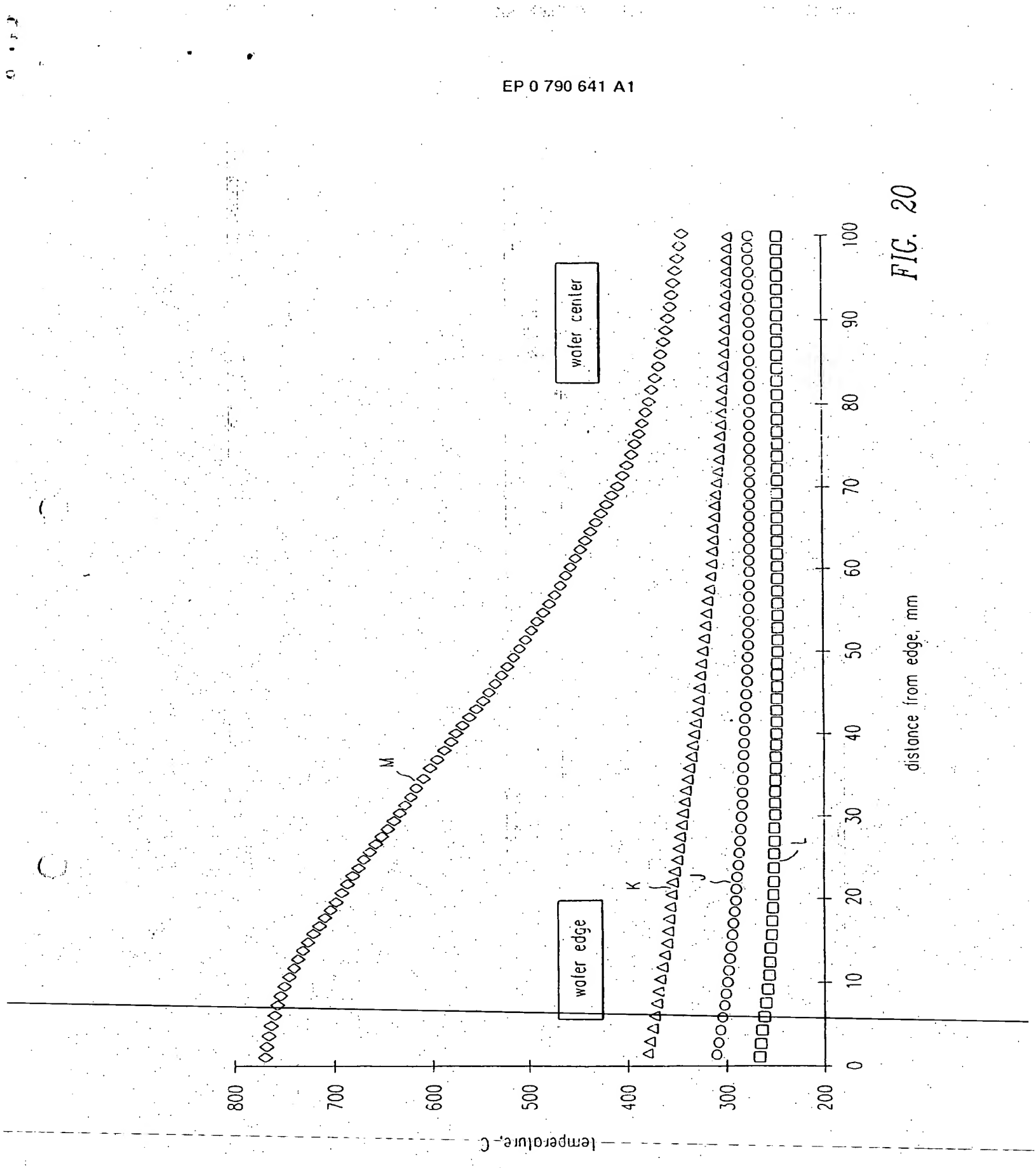
temperature, C
800
700
600
500
400
300
200
0
10
20
30
40
50
60
70
80
90
100
distance from edge, mm
wafer edge
wafer center
M
K
J
L

FIG. 20

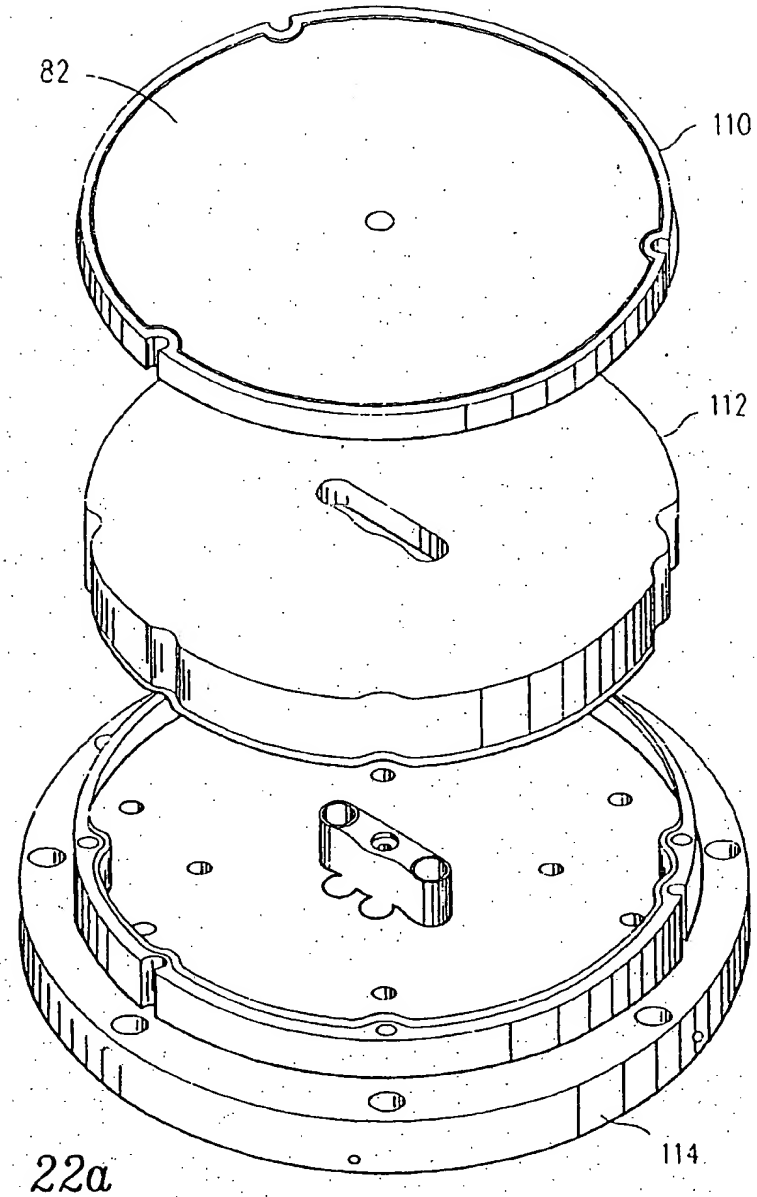

FIG. 22a

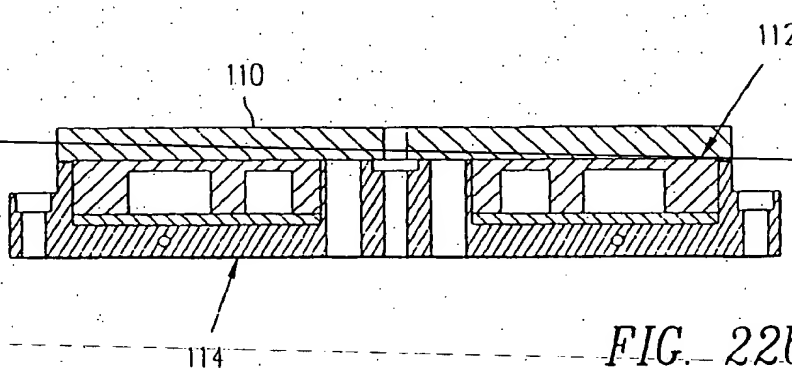

FIG. 22b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 20 0338

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 382 311 A (ISHIKAWA ET AL.) * the whole document *	1,2,26, 27,31, 39-42, 47,50, 68-70	H01L21/00
X	EP 0 644 577 A (HITACHI LTD.) * the whole document *	1,26,27, 30,31, 39,40, 42, 45-47, 68,69	
A	EP 0 488 307 A (TOKYO ELECTRON LIMITED) * the whole document *	1,26,27, 30,39, 40,42, 45-47, 50,68-70	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H01L
C23C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 May 1997	Bolder, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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